

## Z80 CPU V2.01 CONFIGURATION

<b>JP9: ROM pin 26</b>
OFF - Pin 26 == NC (27C64/28C64)
ON - Pin 26 == VCC

<b>JP8: ROM pin 23</b>
1-2 (BOT) - Pin 23 == A11
2-3 (TOP) - Pin 23 == VCC

<b>JP10: ROM Enable</b>
OFF - On-board ROM is disabled
ON - ROM is enabled

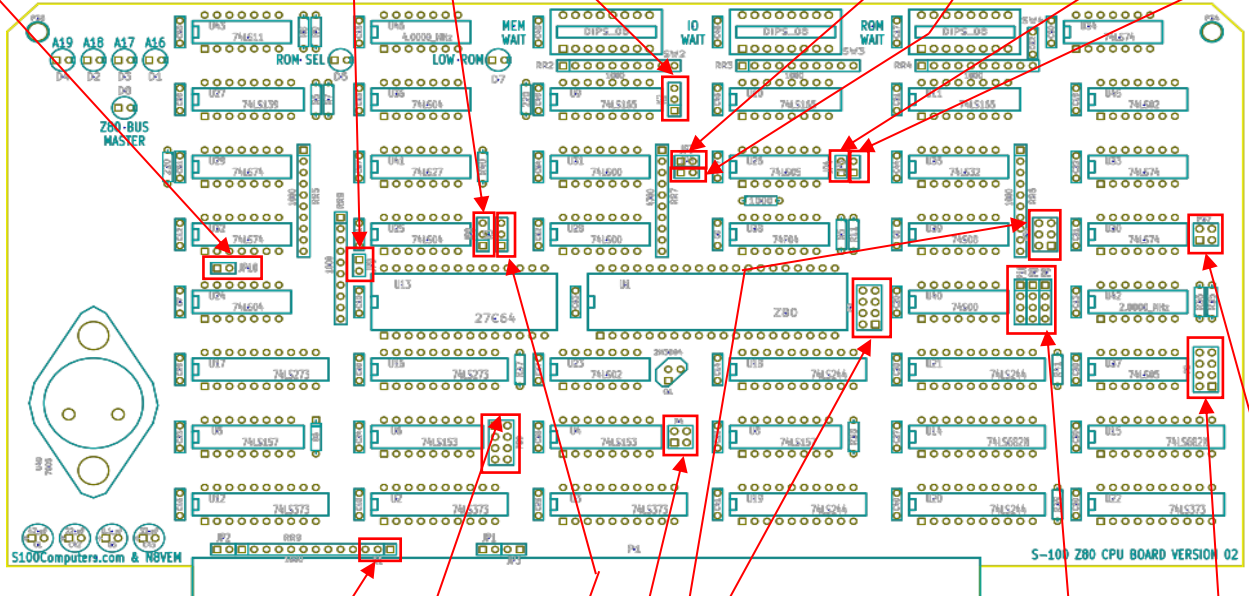
<b>K2: Bus Control Drive</b>
1-2 (BOT) - Non-IEEE, drive conditionally.
2-3 (TOP) - IEEE, drive always while master.

<b>J4: POC* Control</b>
OFF - POC Undriven.
ON - POC driven on power-up

<b>J5: RESET* Capacitor</b>
OFF - RESET* signal as-is
ON - RESET* connected to 33uF cap/1K res.

<b>J6: SLAVE_CLR* Control</b>
OFF - SLAVE_CLR* Undriven.
ON - SLAVE_CLR* driven on power-up

<b>J7: RESET* Control</b>
OFF - RESET* Undriven
ON - RESET* driven on power-up



<b>K1: NMI Connection</b>
1-2 (RIG) - S100 PWRFAIL* pin
2-3 (LEF) - Z80 NMI* pin

<b>P39: ROM pin 2</b>
7-8 (TOP) - pin 2 == IO port 0xD3 bit 1
5-6 - pin 2 == A12
3-4 - pin 2 == GND.
1-2 (BOT) - pin 2 == VCC.

<b>K3: CPU Clock Source</b>
1-2 (BOT) - Local 4MHz oscillator
2-3 (TOP) - S100 NDEF3 pin

<b>P4: CLOCK and MWRT Generation</b>
1-2 (LEF) - Generate 2MHz CLOCK
3-4 (RIG) - Generate MWRT

<b>P36: Wait States</b>
5-6 (TOP) - All memory cycles
3-4 - M1 memory bus cycles
1-2 (BOT) - Every sINTA

<b>P2: Memory Window Configuration Port (DEFAULT=0xD0)</b>
7-8 (TOP) - IO port bit 7
5-6 - IO port bit 6
3-4 - IO port bit 5
1-2 (BOT) - IO port bit 4

<b>P10-P8-P9: Local ROM Address Enable.</b>			
1 (TOP)	A12	L-C: Use A12	C-R: Use 0 OPEN: Use 1
2	A13	L-C: Use A13	C-R: Use 0 OPEN: Use 1
3	A14	L-C: Use A14	C-R: Use 0 OPEN: Use 1
4 (BOT)	A15	L-C: Use A15	C-R: Use 0 OPEN: Use 1

<b>P3: Local ROM Memory Address</b>			
7-8 (TOP)	- A15:	IN=match 0	OUT=match 1
5-6	- A14:	IN=match 0	OUT=match 1
3-4	- A13:	IN=match 0	OUT=match 1
1-2 (BOT)	- A12:	IN=match 0	OUT=match 1

<b>P37: Mode</b>	
1-2 (LEF)	- Partial Latch
3-4 (RIG)	- pSYNC