



> 10. EXAMINE NEXT		
> result: data = 0, addr = 0fffch, status = 0		
> 11. EXAMINE NEXT > result: data = 67b, addr = 0fffbb, status = 0		
> 12. EXAMINE NEXT		
> result: data = 0ffh, addr = 0066h, status = MEMR+M1+/WO		
> result: data = 0ffh. addr = 0067h. status = MEMR+M1+/WO		
> 14. EXAMINE NEXT		
> result: data = 0, addr = 0fffah, status = 0 > and so on until RESET, then it starts over		
>		
> It goes through a similar sequence with DEPOST/DEPOSIT NEXT. I can		
> DEPOSIT, but only if I really have to.		
> If I have valid code at the ZPU's POJ address, it will run just fine if I		
> enable automatic jump and use RESET then RUN.		
> This is exactly how it always behaves, not just sometimes. And it does		
> this whether set to 2 MHz or 4 MHz. None of the wait state options change		
> According to the ZPU manual, you didn't need to do anything special to use		
> this card in an IMSAL. I would suspect the ZPU, but I have a second card > and it behaves exactly the same way. So it's most likely something with		
> the FP, but that works fine with the MPU card. So I'm a bit puzzled here.		
> Hopefully one of you can help.		
> Thanks,		
> Deriver		
Denver,		
change in the EXAMINE NEXT test.) I do have some mods on my front panel -		
check your mods against: http://www.imsai.net/support/cpa_changes.pdf		
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-J -John O O E Reply & Lin with the root may want to check your mods against: http://www.imsai.net/support/cpa_changes.pdf -J -J -John 11/27/2006 11:08:26 PM		
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 check your mods against: http://www.imsai.net/support/cpa_changes.pdf -J -John Image: Solution of the cards of		
 acheck your mods against: http://www.imsai.net/support/cpa_changes.pdf -J John ● ● ■ ■ Repty ▲ John 11/27/2006 11:08:26 PM 		
 check your mods against: http://www.imsai.net/support/cpa_changes.pdf -J -John ● 0 ● ■ Repty & John 11/27/2006 11:08:26 PM 		
check your mods against: http://www.imsai.net/support/cpa_changes.pdf -J -John		
 -J -John O O O O O O O O O O O O O O O O O O O		
 and ogin some form carde and our play for minute. For may want to check your mods against: http://www.imsai.net/support/cpa_changes.pdf John I (2) I (2)		

Microsoft Hosting Experts	Atalasoft
Dedicated ServersASP.NET HostingCloud ServersServer 	
Orcsueb Managed Hosting Solutions	SCAN. VIEW, & ANNOTATE! .NET SDKs to Capture-Enable your applications
It's a variety of timing issues. First, of course, the front designed for the CP-A, which aside from being an 808 But the ZPU can run at 4Mhz (and usually does in mos You may find that if you run it at 2MHz, the problems	panel was), runs at 2MHz. t people's systems). go away.
Second, in some cases hand selection of some of the was necessary to make the board compatible with the	chips on the CP-A ZPU.
Also, some of the operations are controlled by one-sho was controlled by capacitors with a wide tolerance. Se capacitors can also make the CP-A work or not work.	ts whose timing lection of the
It is possible to get a CP-A that works with a ZPU, but automatic. The design of the CP-A was quite marginal	t's not
Actually, there are worse problems (FAR worse) gettin 16FDC to work together. By default, they don't. At all,	g a CP-A and a ever.
Denver Hull wrote:	
> neilo, >	
 > I'm having a little trouble getting a Cromemco ZPU cases > IMSAI 8080. The original MPU-A card works just find 	ard working in my e. The ZPU works in
> a limited way, but front panel operations only work for > cycles after a reset. In other words, after RESET, you	r a couple of u can do a couple
> of EXAMINE/EXAMINE NEXT/DEPOSIT/DEPOSIT I > stop working. Likelieve the EP has all the recommender.	VEXT successfully, then they
 > doesn't matter what other cards are installed, or not in block it bow it behavior with PO L (payor on jump) DI 	nstalled.
 > installed: > 1 power on 	
 > 2. set switches to some address, say 0aaaah > 3. RESET 	
> 4. EXAMINE	Decesh status
 > result. appears to work properly, data = 0ffn, addr = 0 > MEMR+M1+/WO > 5. EXAMINE 	Jaaaan, sialus =
> result: appears to work properly, data = 0ffh, addr = 0 > MEMR+M1+/WO > 6 EXAMUE)aaaah, status =
 > result: doesn't work, data = 0ffh, addr = 0066h, status > 7 EXAMINE 	s = MEMR+M1+/WO
> result: back to addr 0aaaah, status = MEMR+M1+/W > Now it will cycle between the address in the switches	o and 0066b until
 RESET, then it starts over. 	

>	Here's what happens with EXAMINE/EXAMINE NEXT:
>	2. switches = 0aaaah
>	3. RESET
>	result: appears to work, data = 0ffh, addr = 0aaaah, status = MEMR+M1+/WO
>	5. EXAMINE NEXT
>	6. EXAMINE NEXT
>	result: data = 0aah, addr = 0fffeh, status = 0
>	result: data = 0abh, addr = 0fffdh, status = 0
>	8. EXAMINE NEXT
>	9. EXAMINE NEXT
>	result: data = 0ffh, addr = 0067h, status = MEMR+M1+/WO
>	result: data = 0, addr = 0fffch, status = 0
>	11. EXAMINE NEXT result: data = 67b, addr = 0fffbb, status = 0
>	12. EXAMINE NEXT
>	result: data = 0ffh, addr = 0066h, status = MEMR+M1+/WO
>	result: data = 0ffh, addr = 0067h, status = MEMR+M1+/WO
>	14. EXAMINE NEXT result: data = 0. addr = 0fffab. status = 0
>	and so on until RESET, then it starts over.
>	It goes through a similar sequence with DEPOST/DEPOSIT NEXT 1 can
>	correctly deposit data in memory by alternating between RESET, EXAMINE,
>	DEPOSIT, but only if I really have to.
>	I enable automatic jump and use RESET then RUN.
>	This is exactly how it always behaves not just sometimes. And it does
>	this whether set to 2 MHz or 4 MHz. None of the wait state options
>	change this behavior, either.
>	According to the ZPU manual, you didn't need to do anything special to
>	use this card in an IMSAI. I would suspect the ZPU, but I have a second card and it behaves exactly the same way. So it's most likely something
>	with the FP, but that works fine with the MPU card. So I'm a bit
>	puzzled here. Hopefully one of you can help.
>	Thanks,
>	Denver
1	Denver
	WatzmanNOSPAM (5711)
In	and Grane wrote:
JU	
>"	Denver Hull" <denverh@comcast.net> wrote in message</denverh@comcast.net>
>r >	iews:4PednZsbJs2nxPbYnZ2dnUvZ_rednZ2d@comcast.com
>	Halla
>>	>⊓⊂॥∪, >
>>	I'm having a little trouble getting a Cromemco ZPU card working in my
>>	Initial way, but front panel operations only work for a couple of cycles
>>	after a reset. In other words, after RESET, you can do a couple of
>>	>EXAMINE/EXAMINE NEXT/DEPOSIT/DEPOSIT NEXT successfully, then they stop >working. I believe the FP has all the recommended mods. And it doesn't
	· · · · · · · · · · · · · · · · · · ·

>>matter what other cards are installed, or not installed. >>Here is how it behaves with POJ (power on jump) DISABLED, and no memory >>installed: >>1. power on >>2. set switches to some address, say 0aaaah >>3. RESET >>4. EXAMINE >>result: appears to work properly, data = 0ffh, addr = 0aaaah, status = >>MEMR+M1+/WO >>5. EXAMINE >>result: appears to work properly, data = 0ffh, addr = 0aaaah, status = >>MEMR+M1+/WO >>6. EXAMINE >>result: doesn't work, data = 0ffh, addr = 0066h, status = MEMR+M1+/WO >>7. EXAMINE >>result: back to addr 0aaaah, status = MEMR+M1+/WO >>Now it will cycle between the address in the switches and 0066h, until >>RESET, then it starts over. >> >>Here's what happens with EXAMINE/EXAMINE NEXT: >>1. power on >>2. switches = 0aaaah >>3. RESET >>4. EXAMINE >>result: appears to work, data = 0ffh, addr = 0aaaah, status = MEMR+M1+/WO >>5. EXAMINE NEXT >>result: appears to work, data = 0ffh, addr = 0aaabh, status = MEMR+M1+/WO >>6. EXAMINE NEXT >>result: data = 0aah, addr = 0fffeh, status = 0 >>7. EXAMINE NEXT >>result: data = 0abh, addr = 0fffdh, status = 0 >>8. EXAMINE NEXT >>result: data = 0ffh, addr = 0066h, status = MEMR+M1+/WO >>9. EXAMINE NEXT >>result: data = 0ffh, addr = 0067h, status = MEMR+M1+/WO >>10. EXAMINE NEXT >>result: data = 0, addr = 0fffch, status = 0 >>11. EXAMINE NEXT >>result: data = 67h, addr = 0fffbh, status = 0 >>12. EXAMINE NEXT >>result: data = 0ffh, addr = 0066h, status = MEMR+M1+/WO >>13. EXAMINE NEXT >>result: data = 0ffh, addr = 0067h, status = MEMR+M1+/WO >>14. EXAMINE NEXT >>result: data = 0, addr = 0fffah, status = 0 >>and so on until RESET, then it starts over. >> >>It goes through a similar sequence with DEPOST/DEPOSIT NEXT. I can >>correctly deposit data in memory by alternating between RESET, EXAMINE, >>DEPOSIT, but only if I really have to. >>If I have valid code at the ZPU's POJ address, it will run just fine if I >>enable automatic jump and use RESET then RUN. >> >>This is exactly how it always behaves, not just sometimes. And it does >>this whether set to 2 MHz or 4 MHz. None of the wait state options change >>this behavior, either. >> >>According to the ZPU manual, you didn't need to do anything special to use >>this card in an IMSAI. I would suspect the ZPU, but I have a second card >>and it behaves exactly the same way. So it's most likely something with >>the FP, but that works fine with the MPU card. So I'm a bit puzzled here. >>Hopefully one of you can help. >> >>Thanks, >> >>Denver >>

> >Denver,								
 > >I tried your test on my IMSAI 8 >my machine. (Address did not >change in the EXAMINE NEX" >although some RAM cards still >check your mods against: http > 	080 with ZPU. It see change in EXAMINE Γ test.) I do have som I don't play well with ://www.imsai.net/sup	emed to work norma test and status bits ne mods on my fror it. You may want to port/cpa_changes.p	ally on s did not it panel - o odf					
>-J >								
> >-John								
>								
Thanks for the reply John. The RAM cards installed, so I don't document you pointed to is the FP was up to date, but I can ce	system behaves as hink they're a factor. one I used a while ba tainly check again.	described even with I believe the ack to make sure th	n no e					
Thanks,								
Denver								
🔾 o 🤤 🗮	Reply	lenverh (8)	11/28/2006 3:52:56 AM					
Barry Watzman wrote:								
 > It's a variety of timing issues. > was designed for the CP-A, w > 2MHz. But the ZPU can run a > systems). You may find that 	 > It's a variety of timing issues. First, of course, the front panel > was designed for the CP-A, which aside from being an 8080, runs at > 2MHz. But the ZPU can run at 4Mhz (and usually does in most people's > systems). You may find that if you run it at 2MHz, the problems go away. 							
No, it behaves _exactly_ the sa MHz. It also behaves _exactly_ except the FP and the ZPU.	No, it behaves _exactly_ the same way running 2 MHz as it does at 4 MHz. It also behaves _exactly_ the same way when I take out all boards except the FP and the ZPU.							
> > Second, in some cases hand > was necessary to make the b	 Second, in some cases hand selection of some of the chips on the CP-A was necessary to make the board compatible with the ZPU. 							
Any suggestions about which ones, or what to look for?								
 > Also, some of the operations > was controlled by capacitors > capacitors can also make the 	 > > Also, some of the operations are controlled by one-shots whose timing > was controlled by capacitors with a wide tolerance. Selection of the > capacitors can also make the CP-A work or not work. 							
So I have heard, but then I wou (or not work) one way, others a (mis)behave exactly the same w twice after a RESET, then misb followed by a DEPOSIT or EXA they don't - until I RESET again the one-shots on the FP and the one-shots are a possability, but	So I have heard, but then I would almost expect some functions to work (or not work) one way, others another. In this case, all functions (mis)behave exactly the same way. On top of that, they all always work twice after a RESET, then misbehave. I can do a RESET, then an EXAMINE followed by a DEPOSIT or EXAMINE NEXT, and those two work. After that they don't - until I RESET again. I don't see any connection between the one-shots on the FP and the RESET switch. I admit that the one-shots are a possability, but it doesn't sound likely.							
Any ideas about what the timing	Any ideas about what the timings should be, in case I want to persue that?							
> > It is possible to get a CP-A th	at works with a ZPU,	but it's not						

> auton	natic. The	design c	of the CP-A was	quite marginal.		
>		u e e i g i i e		quite maiginan		
> Actua > 16FD	lly, there a C to work	together.	e problems (FAF . By default, the	R worse) getting a CP-A ey don't. At all, ever.	and a	
l've hea I'm not	ard that, too going to w	o. Fortur orry abou	nately, I'm not tr ut that one.	ying to use a 16FDC, so	0	
Thanks	3					
Denver						
0	D 🗢		Reply	denverh (8)	11/28/2006 4:05:11 AM	
Dam						
>>Den	/er,					
>>I trie	d your test	on my II	MSAI 8080 with	ZPU. It seemed to wor	k normally	
>>on m	y machine hange in t	he EXAN	ss did not chang IINE NEXT test	.) I do have some mods	on my front	
>>pane	l - althoug	gh some	RAM cards still	don't play well with it. ১	You may	
>>want	to check y	/our mod ai net/su	ls against: poort/cpa_chan	nes ndf		
>> >>	/	1.1107.001	opon/opa_onan	geo.pui		
>>-J						
>>						
>>						
>>-Johr	ר					
>>						
> Than	ks for the r	eply Joh	n. The system	behaves as described e	even with no	
> RAM	cards insta	alled, so	I don't think the	y're a factor. I believe ti ed a while back to make	he A sure the FP	
> was u	ip to date,	but I can	certainly check	again.		
>	· ·		-	•		
> Than	KS,					
> Denv	er					
Denver	3					
l pulled test cor	the memo ditions.	ory card v	vhen I ran the te	est, as I tried to duplicate	e your	
The tex	t: "some F	RAM care	ds still don't play	/ well with it" refers to R	AM	
cards n confusi	ot playing on.	well with	the front panel	not the ZPU. Sorry ab	out the	
I mentio	oned RAM	cards be	cause it's the o	nly known incompatibilit	ty with my	
system	when runr	ning norn	nally. In particu	ular, later cards don't wo	ork with	
the FP.	i normally	/ run with emco 16	ו נחפ ∠PU, a Co KPR holding mv	mpupro RAM17, an IMS / monitor in FPROM In	או טט serial hthis setup, the	
FP is u	seless - alt	hough p	ower on jump g	ets me to the monitor.	But if I	
swap o	ut the RAN	117 for a	n earlier card - I	ike a genuine IMSAI 4K	, the FP	
works. avail. I	suspect th	ne CPA le proble	(rr) = 0.0 for the m is due to a di	fference between the	Calus, IO IIO	
"Altair/I	MSAI" bus	and the	IEEE 696 bus s	standard. I just haven't	had the	
time (or	desire) to	pull it all	apart again as	it does work for what I r	need.	
With re	gard to the	other th	read about one	shots - this is true, they	r can get	
flakey.	It may be	that the	waveforms gene	erated are just within to	erance of	
the 808 replace	o mpu, bu compone	τ cause p nts on th	e FP. 74xx chir	e ∠ou. It may save time and caps are cheap -	e to just much cheaper	
than yo	u spending	g days so	cratching your h	ead.		

-J				
-J				
0				
🔾 o 🤤	Reply	⁸ John	11/28/2006 7:18:34 AM	
Denver Hull wrote:				
<snip> > Thanks,</snip>				
> > Denver				
Hi Denver,				
Looking at the add check the wiring of	ress the Z80 jumps to, (⁻ the Z80 NMI line.	0x0066, I would especiall	/	
0x0066 is the NMI	restart address. Perhap	s it sees an NMI.		
Regards,				
Hans Bus				
🗘 o 🤤	Reply	thisis (6)	11/28/2006 8:13:35 AM	
		()		
Hi,			Dec	
Disk 1 + Ram17.	2PU together with no is:	sues along with Compu	Pro	
I started with an also had to modify	unmodified CPA, did sou	ne but not all the mods.	l na the	
Mwrite signal, and ZPU to not generat	that card should be the te Mwrite I lifted a pin	CPA. Make sure to mod on one of the chips.	l the	
~ J				
Denver Hull wrote: > I'm having a little	trouble getting a Crome	emco ZPU card working i	ו my	
> IMSAI 8080.				
0.0	and a			_
V 0 V	🚍 Reply	🛲 jsnospam (141)	11/28/2006 4:17:04 PM	
Hans Bus wrote:				
> Denver Hull wrot > <snip></snip>	e:			
> >> Thanks,				
>>				

>> Denver						
>						
> > Hi Denver,						
> > Looking at the address the Z80 jumps to, 0x0066, I would especially > check the wiring of the Z80 NMI line. >						
> 0x0066 is the NMI restart address. Perhaps it sees an NMI.						
 > Regards, > Hans Bus 						
Hah! That was the clue! One of the FP mods, for MPU-B compatibility, calls for a connection between S-100 bus pins 3 and 12. That ends up connecting XRDY (FP processor control) to the ZPU NMI input. The MPU-A doesn't use pin 12, so it didn't bother that card, but it sure made the ZPU act strange. Of course this mod is under the switch support bar, so it's hard to see, and harder to get at. But I took it out, and everything works just fine now.						
Thanks all,						
Denver						
 O ○ E Reply Centre (8) 11/28/2006 5:24:23 PM ■ 						
jsnospam@cimmeri.com wrote: >Hi, > I run a CPA and ZPU together with no issues along with CompuPro >Disk 1 + Ram17. > I started with an unmodified CPA, did some but not all the mods. I >also had to modify the ZPU since only one card should be generating the >Mwrite signal, and that card should be the CPA. Make sure to mod the >ZPU to not generate Mwrite I lifted a pin on one of the chips. > "Some but not all the modes" is significant. As it happened, the mod for MPU-B was installed, which connected XRDY to the ZPU NMI. After I removed that one, things improved dramatically. I'll check that MWRITE signal though. That's a good tip. Thanks, Denver						
Thanks, Denver						
Thanks, Denver						
Thanks, Denver						
Thanks, Denver						
Thanks, Denver						
Thanks, Denver						
Thanks, Denver						
Thanks, Denver						