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Jameco Part Number 2059356

## Real-Time Clock

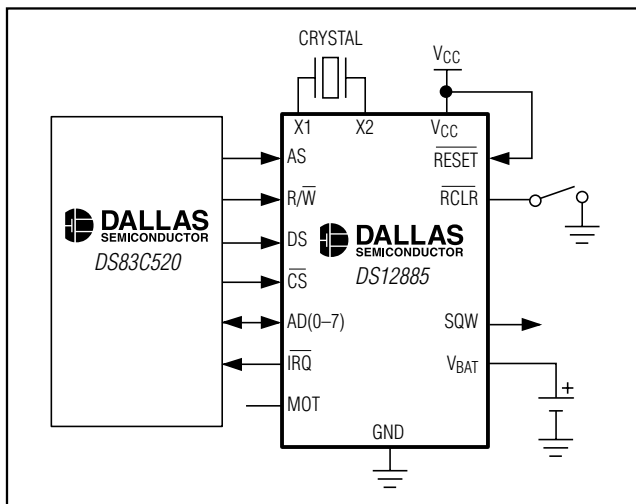
### General Description

The DS12885, DS12887, and DS12C887 real-time clocks (RTCs) are designed to be direct replacements for the DS1285 and DS1287. The devices provide a real-time clock/calendar, one time-of-day alarm, three maskable interrupts with a common interrupt output, a programmable square wave, and 114 bytes of battery-backed static RAM (113 bytes in the DS12C887 and DS12C887A). The DS12887 integrates a quartz crystal and lithium energy source into a 24-pin encapsulated DIP package. The DS12C887 adds a century byte at address 32h. For all devices, the date at the end of the month is automatically adjusted for months with fewer than 31 days, including correction for leap years. The devices also operate in either 24-hour or 12-hour format with an AM/PM indicator. A precision temperature-compensated circuit monitors the status of VCC. If a primary power failure is detected, the device automatically switches to a backup supply. A lithium coin-cell battery can be connected to the VBAT input pin on the DS12885 to maintain time and date operation when primary power is absent. The device is accessed through a multiplexed byte-wide interface, which supports both Intel and Motorola modes.

### Applications

Embedded Systems  
Utility Meters  
Security Systems  
Network Hubs, Bridges, and Routers

### Typical Operating Circuit



Pin Configurations and Ordering Information appear at end of data sheet.

### Features

- ◆ Drop-In Replacement for IBM AT Computer Clock/Calendar
- ◆ RTC Counts Seconds, Minutes, Hours, Day, Date, Month, and Year with Leap Year Compensation Through 2099
- ◆ Binary or BCD Time Representation
- ◆ 12-Hour or 24-Hour Clock with AM and PM in 12-Hour Mode
- ◆ Daylight Saving Time Option
- ◆ Selectable Intel or Motorola Bus Timing
- ◆ Interfaced with Software as 128 RAM Locations
- ◆ 14 Bytes of Clock and Control Registers
- ◆ 114 Bytes of General-Purpose, Battery-Backed RAM (113 Bytes in the DS12C887 and DS12C887A)
- ◆ RAM Clear Function (DS12885, DS12887A, and DS12C887A)
- ◆ Interrupt Output with Three Independently Maskable Interrupt Flags
- ◆ Time-of-Day Alarm Once Per Second to Once Per Day
- ◆ Periodic Rates from 122 $\mu$ s to 500ms
- ◆ End-of-Clock Update Cycle Flag
- ◆ Programmable Square-Wave Output
- ◆ Automatic Power-Fail Detect and Switch Circuitry
- ◆ Optional 28-Pin PLCC Surface Mount Package or 32-Pin TQFP (DS12885)
- ◆ Optional Encapsulated DIP (EDIP) Package with Integrated Crystal and Battery (DS12887, DS12887A, DS12C887, DS12C887A)
- ◆ Optional Industrial Temperature Range Available
- ◆ Underwriters Laboratory (UL) Recognized

# Real-Time Clock

## ABSOLUTE MAXIMUM RATINGS

Voltage Range on V<sub>CC</sub> Pin Relative to Ground .....-0.3V to +6.0V  
 Operating Temperature Range .....  
     Commercial (noncondensing) .....0°C to +70°C  
 Operating Temperature Range .....  
     Industrial (noncondensing).....-40°C to +85°C

Storage Temperature Range .....-55°C to +125°C  
 Soldering Temperature .....See IPC/JEDEC  
     J-STD-020 Specification (Note 1)  
 Soldering Temperature (leads, 10s).....+260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## DC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = +4.5V to +5.5V, T<sub>A</sub> = over the operating range, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V <sub>CC</sub>	(Note 3)	4.5		5.5	V
V <sub>BAT</sub> Input Voltage	V <sub>BAT</sub>	(Note 3)	2.5		4.0	V
Input Logic 1	V <sub>IH</sub>	(Note 3)	2.2		V <sub>CC</sub> + 0.3	V
Input Logic 0	V <sub>IL</sub>	(Note 3)	-0.3		+0.8	V
V <sub>CC</sub> Power-Supply Current	I <sub>CC1</sub>	(Note 4)			15	mA
V <sub>CC</sub> Standby Current	I <sub>CCS</sub>	(Note 5)				mA
Input Leakage	I <sub>IL</sub>		-1.0		+1.0	μA
I/O Leakage	I <sub>OL</sub>	(Note 6)	-1.0		+1.0	μA
Input Current	I <sub>MOT</sub>	(Note 7)	-1.0		+500	μA
Output at 2.4V	I <sub>OH</sub>	(Note 3)	-1.0			mA
Output at 0.4V	I <sub>OL</sub>	(Note 3)			4.0	mA
Power-Fail Voltage	V <sub>PF</sub>	(Note 3)	4.0	4.25	4.5	V
VRT Trip Point	VRT <sub>TRIP</sub>			1.3		V

# Real-Time Clock

## DC ELECTRICAL CHARACTERISTICS

( $V_{CC} = 0V$ ,  $V_{BAT} = 3.0V$ ,  $T_A$  = over the operating range, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{BAT}$ Current (OSC On); $T_A = +25^\circ C$ , $V_{BACKUP} = 3.0V$	$I_{BAT}$	(Note 8)			500	nA
$V_{BAT}$ Current (Oscillator Off)	$I_{BATDR}$	(Note 8)			100	nA

## AC ELECTRICAL CHARACTERISTICS

( $V_{CC} = 4.5V$  to  $5.5V$ ,  $T_A$  = over the operating range.) (Note 2)

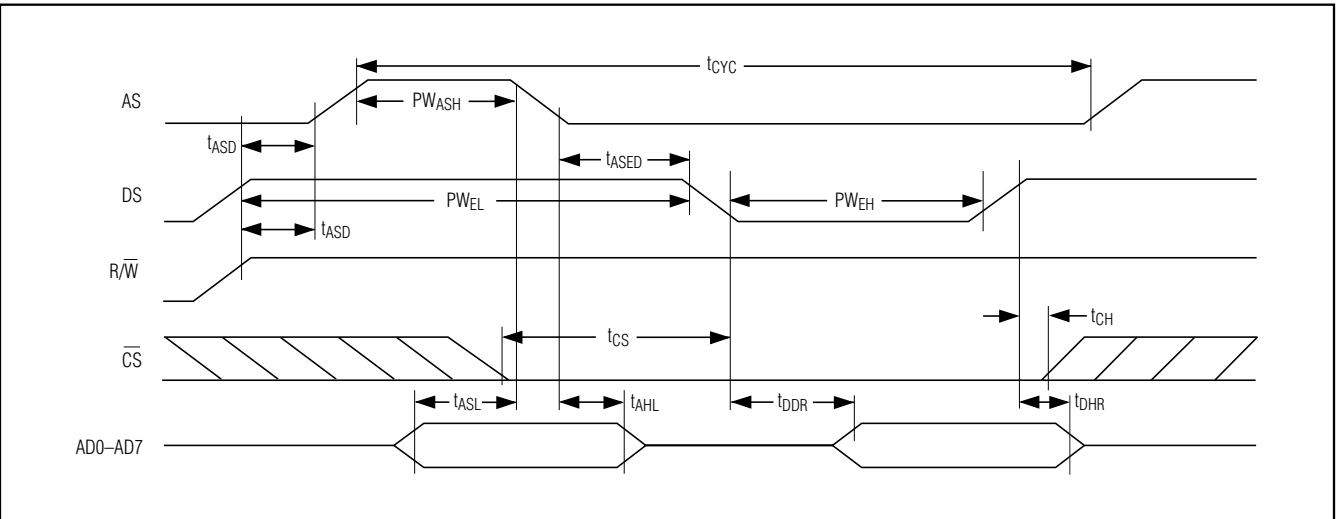
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Cycle Time	$t_{CYC}$		385		DC	ns
Pulse Width, DS Low or $R/\bar{W}$ High	$PW_{EL}$		150			ns
Pulse Width, DS High or $R/\bar{W}$ Low	$PW_{EH}$		125			ns
Input Rise and Fall	$t_R, t_F$				30	ns
$R/\bar{W}$ Hold Time	$t_{RWH}$		10			ns
$R/\bar{W}$ Setup Time Before DS/E	$t_{RWS}$		50			ns
Chip-Select Setup Time Before DS or $R/\bar{W}$	$t_{CS}$		20			ns
Chip-Select Hold Time	$t_{CH}$		0			ns
Read-Data Hold Time	$t_{DHR}$		10		80	ns
Write-Data Hold Time	$t_{DHW}$		0			ns
Address Valid Time to AS Fall	$t_{ASL}$		30			ns
Address Hold Time to AS Fall	$t_{AHL}$		10			ns
Delay Time DS/E to AS Rise	$t_{ASD}$		20			ns
Pulse Width AS High	$PW_{ASH}$		60			ns
Delay Time, AS to DS/E Rise	$t_{ASED}$		40			ns
Output Data Delay Time from DS or $R/\bar{W}$	$t_{DDR}$		20		120	ns
Data Setup Time	$t_{DSW}$		100			ns
Reset Pulse Width	$t_{RWL}$		5			$\mu s$
$\overline{IRQ}$ Release from DS	$t_{IRDS}$				2	$\mu s$
$\overline{IRQ}$ Release from $\overline{RESET}$	$t_{IRR}$				2	$\mu s$

DS12885/DS12887/DS12887A/DS12C887/DS12C887A

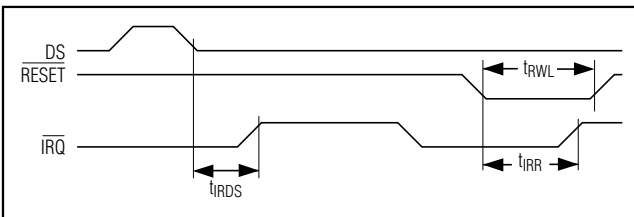


# Real-Time Clock

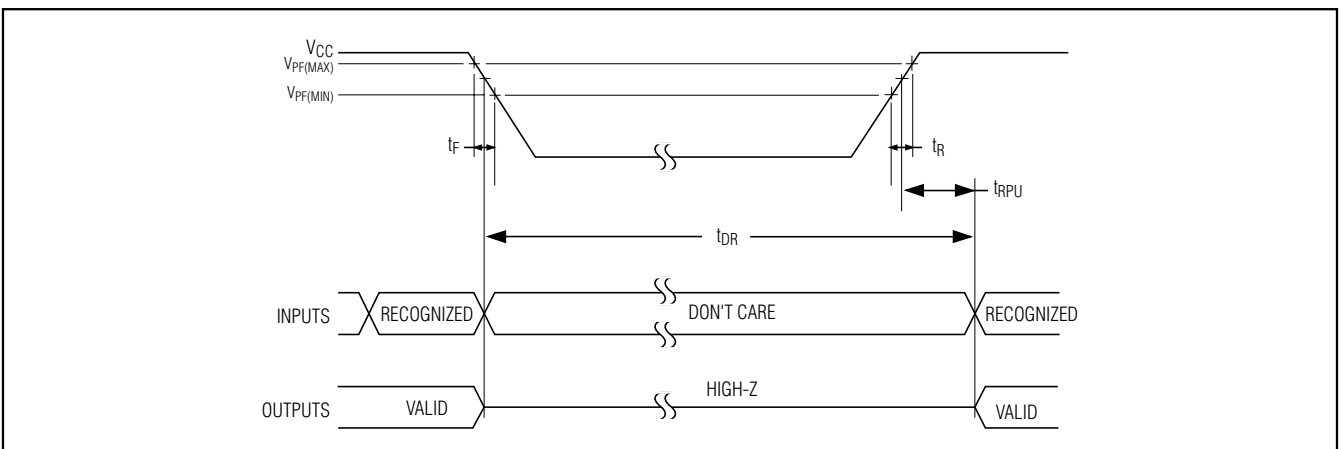
## Intel Bus Read Timing



## IRQ Release Delay Timing



## Power-Up/Power-Down Timing



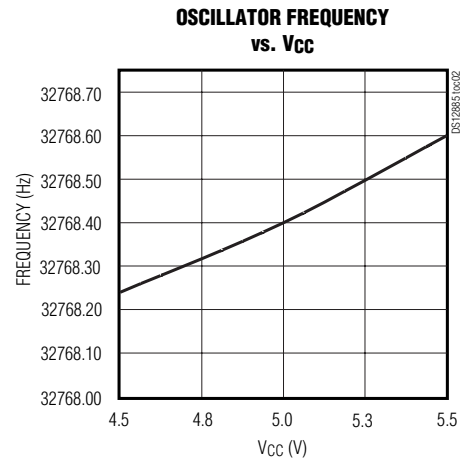
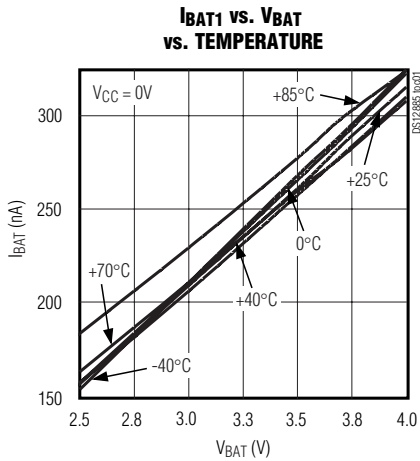
DS12885/DS12887/DS12887A/DS12C887/DS12C887A



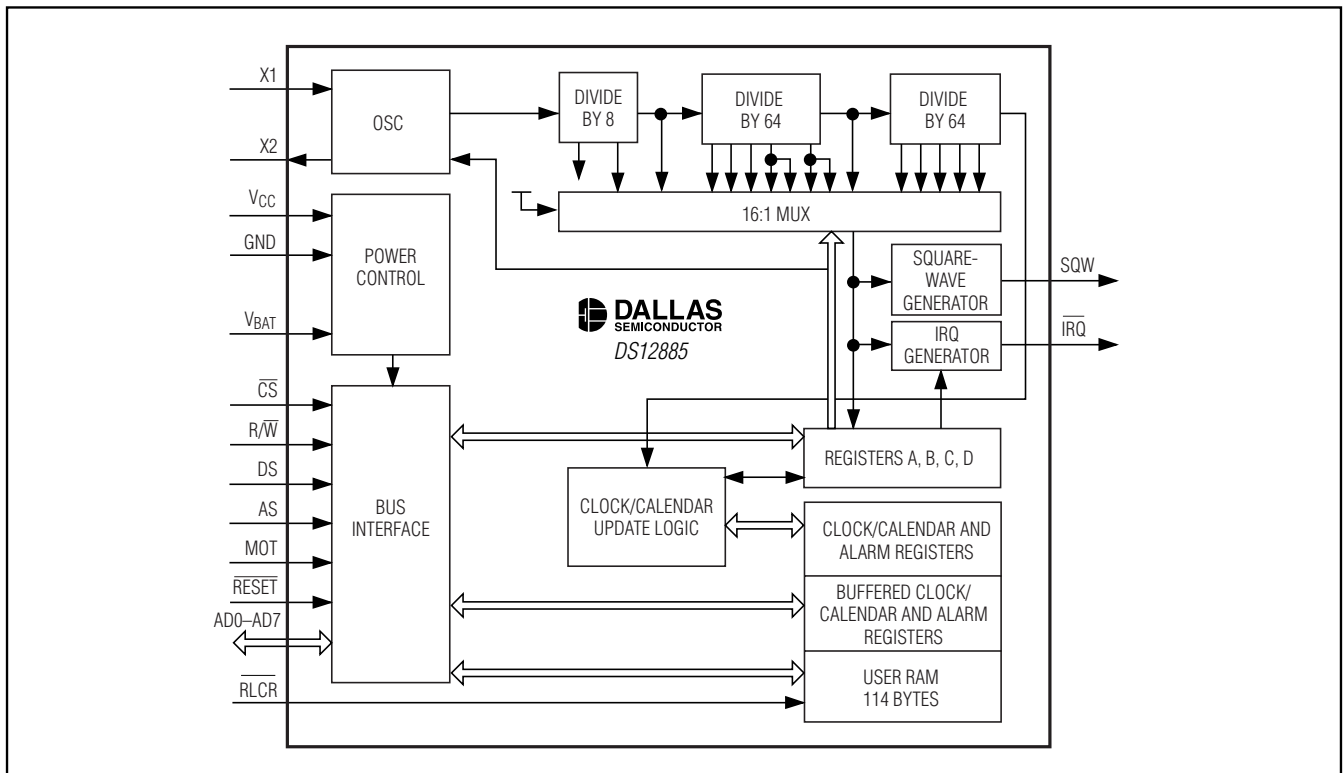
# Real-Time Clock

## Typical Operating Characteristics

( $V_{CC} = +5.0V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



## Functional Diagram



DS12885/DS12887/DS12887A/DS12C887/DS12C887A



# Real-Time Clock

## Pin Description

PIN				NAME	FUNCTION
SO, PDIP	EDIP	PLCC	TQFP		
1	1	2	29	MOT	Motorola or Intel Bus Timing Selector. This pin selects one of two bus types. When connected to V <sub>CC</sub> , Motorola bus timing is selected. When connected to GND or left disconnected, Intel bus timing is selected. The pin has an internal pulldown resistor.
2	—	3	30	X1	Connections for Standard 32.768kHz Quartz Crystal. The internal oscillator circuitry is designed for operation with a crystal having a 6pF specified load capacitance (C <sub>L</sub> ). Pin X1 is the input to the oscillator and can optionally be connected to an external 32.768kHz oscillator. The output of the internal oscillator, pin X2, is floated if an external oscillator is connected to pin X1.
3	—	4	31	X2	
4–11	4–11	5–10, 12, 14	1, 2, 3, 5, 7, 8, 9, 11	AD0–AD7	Multiplexed, Bidirectional Address/Data Bus. The addresses are presented during the first portion of the bus cycle and latched into the device by the falling edge of AS. Write data is latched by the falling edge of DS (Motorola timing) or the rising edge of R <sub>W</sub> (Intel timing). In a read cycle, the device outputs data during the latter portion of DS (DS and R <sub>W</sub> high for Motorola timing, DS low and R <sub>W</sub> high for Intel timing). The read cycle is terminated and the bus returns to a high-impedance state as DS transitions low in the case of Motorola timing or as DS transitions high in the case of Intel timing.
12, 16	12	15, 20	12, 17	GND	Ground
13	13	16	13	$\overline{CS}$	Active-Low Chip-Select Input. The chip-select signal must be asserted low for a bus cycle in the device to be accessed. $\overline{CS}$ must be kept in the active state during DS and AS for Motorola timing and during DS and R <sub>W</sub> for Intel timing. Bus cycles that take place without asserting $\overline{CS}$ will latch addresses, but no access occurs. When V <sub>CC</sub> is below V <sub>PF</sub> volts, the device inhibits access by internally disabling the $\overline{CS}$ input. This action protects the RTC data and the RAM data during power outages.
14	14	17	14	AS	Address Strobe Input. A positive-going address-strobe pulse serves to demultiplex the bus. The falling edge of AS causes the address to be latched within the device. The next rising edge that occurs on the AS bus clears the address regardless of whether $\overline{CS}$ is asserted. An address strobe must immediately precede each write or read access. If a write or read is performed with $\overline{CS}$ deasserted, another address strobe must be performed prior to a read or write access with $\overline{CS}$ asserted.
15	15	19	16	R <sub>W</sub>	Read/Write Input. The R <sub>W</sub> pin has two modes of operation. When the MOT pin is connected to V <sub>CC</sub> for Motorola timing, R <sub>W</sub> is at a level that indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on R <sub>W</sub> while DS is high. A write cycle is indicated when R <sub>W</sub> is low during DS. When the MOT pin is connected to GND for Intel timing, the R <sub>W</sub> signal is an active-low signal. In this mode, the R <sub>W</sub> pin operates in a similar fashion as the write-enable signal ( $\overline{WE}$ ) on generic RAMs. Data are latched on the rising edge of the signal.

# Real-Time Clock

## Pin Description (continued)

PIN				NAME	FUNCTION
SO, PDIP	EDIP	PLCC	TQFP		
22	2, 3, 16, 20, 21, 22	1, 11, 13, 18, 26	4, 6, 10, 15, 20, 23, 25, 27, 32	N.C.	No Connection. This pin should remain unconnected. Pin 21 is $\overline{RCLR}$ for the DS12887A/DS12C887A. On the EDIP, these pins are missing by design.
17	17	21	18	DS	Data Strobe or Read Input. The DS pin has two modes of operation depending on the level of the MOT pin. When the MOT pin is connected to $V_{CC}$ , Motorola bus timing is selected. In this mode, DS is a positive pulse during the latter portion of the bus cycle and is called data strobe. During read cycles, DS signifies the time that the device is to drive the bidirectional bus. In write cycles, the trailing edge of DS causes the device to latch the written data. When the MOT pin is connected to GND, Intel bus timing is selected. DS identifies the time period when the device drives the bus with read data. In this mode, the DS pin operates in a similar fashion as the output-enable ( $\overline{OE}$ ) signal on a generic RAM.
18	18	22	19	$\overline{RESET}$	Active-Low Reset Input. The $\overline{RESET}$ pin has no effect on the clock, calendar, or RAM. On power-up, the $\overline{RESET}$ pin can be held low for a time to allow the power supply to stabilize. The amount of time that $\overline{RESET}$ is held low is dependent on the application. However, if $\overline{RESET}$ is used on power-up, the time $\overline{RESET}$ is low should exceed 200ms to ensure that the internal timer that controls the device on power-up has timed out. When $\overline{RESET}$ is low and $V_{CC}$ is above $V_{PF}$ , the following occurs: <ul style="list-style-type: none"> <li>A. Periodic interrupt-enable (PIE) bit is cleared to 0.</li> <li>B. Alarm interrupt-enable (AIE) bit is cleared to 0.</li> <li>C. Update-ended interrupt-enable (UIE) bit is cleared to 0.</li> <li>D. Periodic-interrupt flag (PF) bit is cleared to 0.</li> <li>E. Alarm-interrupt flag (AF) bit is cleared to 0.</li> <li>F. Update-ended interrupt flag (UF) bit is cleared to 0.</li> <li>G. Interrupt-request status flag (IRQF) bit is cleared to 0.</li> <li>H. <math>\overline{IRQ}</math> pin is in the high-impedance state.</li> <li>I. The device is not accessible until <math>\overline{RESET}</math> is returned high.</li> <li>J. Square-wave output-enable (SQWE) bit is cleared to 0.</li> </ul> In a typical application, $\overline{RESET}$ can be connected to $V_{CC}$ . This connection allows the device to go in and out of power fail without affecting any of the control registers.

DS12885/DS12887/DS12887A/DS12C887/DS12C887A

## Real-Time Clock

### Pin Description (continued)

PIN				NAME	FUNCTION
SO, PDIP	EDIP	PLCC	TQFP		
19	19	23	21	$\overline{\text{IRQ}}$	Active-Low Interrupt Request Output. The $\overline{\text{IRQ}}$ pin is an active-low output of the device that can be used as an interrupt input to a processor. The $\overline{\text{IRQ}}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. The processor program normally reads the C register to clear the $\overline{\text{IRQ}}$ pin. The $\overline{\text{RESET}}$ pin also clears pending interrupts. When no interrupt conditions are present, the $\overline{\text{IRQ}}$ level is in the high-impedance state. Multiple interrupting devices can be connected to an $\overline{\text{IRQ}}$ bus, provided that they are all open drain. The $\overline{\text{IRQ}}$ pin is an open-drain output and requires an external pullup resistor to $V_{CC}$ .
20	—	24	22	$V_{BAT}$	Connection for a Primary Battery. (DS12885 Only.) Battery voltage must be held between the minimum and maximum limits for proper operation. If a backup supply is not supplied, $V_{BAT}$ must be grounded. Connect the battery directly to the $V_{BAT}$ pin. Diodes in series between the $V_{BAT}$ pin and the battery may prevent proper operation. UL recognized to ensure against reverse charging when used with a lithium battery.
21	21 (DS12887A/ DS12C887A)	25	24	$\overline{\text{RCLR}}$	Active-Low RAM Clear. The $\overline{\text{RCLR}}$ pin is used to clear (set to logic 1) all the general-purpose RAM, but does not affect the RAM associated with the RTC. To clear the RAM, $\overline{\text{RCLR}}$ must be forced to an input logic 0 during battery-backup mode when $V_{CC}$ is not applied. The $\overline{\text{RCLR}}$ function is designed to be used through a human interface (shorting to ground manually or by a switch) and not to be driven with external buffers. This pin is internally pulled up. Do not use an external pullup resistor on this pin.
23	23	27	26	SQW	Square-Wave Output. The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the RTC. The frequency of the SQW pin can be changed by programming Register A, as shown in Table 1. The SQW signal can be turned on and off using the SQWE bit in Register B. The SQW signal is not available when $V_{CC}$ is less than $V_{PF}$ .
24	24	28	28	$V_{CC}$	DC Power Pin for Primary Power Supply. When $V_{CC}$ is applied within normal limits, the device is fully accessible and data can be written and read. When $V_{CC}$ is below $V_{PF}$ reads and writes are inhibited.

# Real-Time Clock

## Detailed Description

The DS12885 family of RTCs provide 14 bytes of real-time clock/calendar, alarm, and control/status registers and 114 bytes (113 bytes for DS12C887 and DS12C887A) of nonvolatile, battery-backed static RAM. A time-of-day alarm, three maskable interrupts with a common interrupt output, and a programmable square-wave output are available. The devices also operate in either 24-hour or 12-hour format with an AM/PM indicator. A precision temperature-compensated circuit monitors the status of VCC. If a primary power-supply failure is detected, the devices automatically switch to a backup supply. The backup supply input supports a primary battery, such as lithium coin cell. The devices are accessed through a multiplexed address/data bus that supports Intel and Motorola modes.

## Oscillator Circuit

The DS12885 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Table 1 specifies several crystal parameters for the external crystal. Figure 1 shows a functional schematic of the oscillator circuit. An enable bit in the control register controls the oscillator. Oscillator startup times are highly dependent upon crystal characteristics, PC board leakage, and layout. High ESR and excessive capacitive loads are the major contributors to long startup times. A circuit using a crystal with the recommended characteristics and proper layout usually starts within one second.

An external 32.768kHz oscillator can also drive the DS12885. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.

Table 1. Crystal Specifications\*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	$f_0$		32.768		kHz
Series Resistance	ESR			50	$k\Omega$
Load Capacitance	$C_L$		6		pF

\*The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to Application Note 58: Crystal Considerations for Dallas Real-Time Clocks for additional specifications.

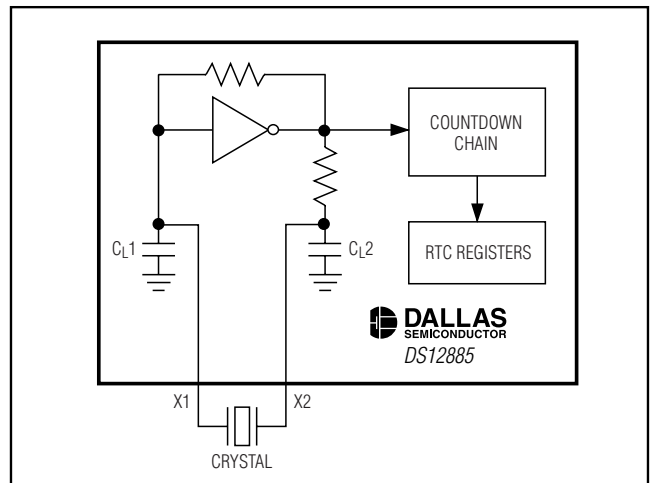


Figure 1. Oscillator Circuit Showing Internal Bias Network

DS12885/DS12887/DS12887A/DS12C887/DS12C887A



# Real-Time Clock

The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day, if the alarm-enable bit is high. In this mode, the “0” bits in the alarm registers and the corresponding time registers must always be written to 0 (Table 2A and 2B). Writing the 0 bits in the alarm and/or time registers to 1 can result in undefined operation.

The second use condition is to insert a “don’t care” state in one or more of the three alarm bytes. The don’t-care code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the don’t-care

condition when at logic 1. An alarm is generated each hour when the don’t-care bits are set in the hours byte. Similarly, an alarm is generated every minute with don’t-care codes in the hours and minute alarm bytes. The don’t-care codes in all three alarm bytes create an interrupt every second.

All 128 bytes can be directly written or read, except for the following:

- 1) Registers C and D are read-only.
- 2) Bit 7 of register A is read-only.
- 3) The MSB of the seconds byte is read-only.

**Table 2A. Time, Calendar, and Alarm Data Modes—BCD Mode (DM = 0)**

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
00H	0	10 Seconds			Seconds				Seconds	00–59
01H	0	10 Seconds			Seconds				Seconds Alarm	00–59
02H	0	10 Minutes			Minutes				Minutes	00–59
03H	0	10 Minutes			Minutes				Minutes Alarm	00–59
04H	AM/PM	0	0	10 Hours	Hours				Hours	1–12 +AM/PM 00–23
	0		10 Hours							
05H	AM/PM	0	0	10 Hours	Hours				Hours Alarm	1–12 +AM/PM 00–23
	0		10 Hours							
06H	0	0	0	0	0	Day			Day	01–07
07H	0	0	10 Date		Date				Date	01–31
08H	0	0	0	10 Months	Month				Month	01–12
09H	10 Years				Year				Year	00–99
0AH	UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0	Control	—
0BH	SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE	Control	—
0CH	IRQF	PF	AF	UF	0	0	0	0	Control	—
0DH	VRT	0	0	0	0	0	0	0	Control	—
0EH-31H	X	X	X	X	X	X	X	X	RAM	—
32H	10 Century				Century				Century*	00–99
33H-7FH	X	X	X	X	X	X	X	X	RAM	—

X = Read/Write Bit.

\*DS12C887, DS12C887A only. General-purpose RAM on DS12885, DS12887, and DS12887A.

**Note:** Unless otherwise specified, the state of the registers is not defined when power is first applied. Except for the seconds register, 0 bits in the time and date registers can be written to 1, but may be modified when the clock updates. 0 bits should always be written to 0 except for alarm mask bits.

## Real-Time Clock

**Table 2B. Time, Calendar, and Alarm Data Modes—Binary Mode (DM = 1)**

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
00H	0	0	Seconds						Seconds	00–3B
01H	0	0	Seconds						Seconds Alarm	00–3B
02H	0	0	Minutes						Minutes	00–3B
03H	0	0	Minutes						Minutes Alarm	00–3B
04H	AM/PM	0	0	0	Hours				Hours	01–0C +AM/PM 00–17
	0			Hours						
05H	AM/PM	0	0	0	Hours				Hours Alarm	01–0C +AM/PM 00–17
	0			Hours						
06H	0	0	0	0	0	Day		Day	01–07	
07H	0	0	0	Date				Date	01–1F	
08H	0	0	0	0	Month				Month	01–0C
09H	0	Year						Year	00–63	
0AH	UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0	Control	—
0BH	SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE	Control	—
0CH	IRQF	PF	AF	UF	0	0	0	0	Control	—
0DH	VRT	0	0	0	0	0	0	0	Control	—
0EH–31H	X	X	X	X	X	X	X	X	RAM	—
32H	N/A				N/A				Century*	—
33H–7FH	X	X	X	X	X	X	X	X	RAM	—

X = Read/Write Bit.

\*DS12C887, DS12C887A only. General-purpose RAM on DS12885, DS12887, and DS12887A.

**Note:** Unless otherwise specified, the state of the registers is not defined when power is first applied. Except for the seconds register, 0 bits in the time and date registers can be written to 1, but may be modified when the clock updates. 0 bits should always be written to 0 except for alarm mask bits.

# Real-Time Clock

## Control Registers

The real-time clocks have four control registers that are accessible at all times, even during the update cycle.

### Control Register A

MSB				LSB			
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

**Bit 7: Update-In-Progress (UIP).** This bit is a status flag that can be monitored. When the UIP bit is a 1, the update transfer occurs soon. When UIP is a 0, the update transfer does not occur for at least 244 $\mu$ s. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is 0. The UIP bit is read-only and is not affected by  $\overline{\text{RESET}}$ . Writing the SET bit in Register B to a 1 inhibits any update transfer and clears the UIP status bit.

**Bits 6, 5, and 4: DV2, DV1, DV0.** These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits that turn the oscillator on and allow the RTC to keep time. A pattern of 11x enables the oscillator but holds the countdown chain in reset. The next update occurs at 500ms after a pattern of 010 is written to DV0, DV1, and DV2.

**Bits 3 to 0: Rate Selector (RS3, RS2, RS1, RS0).** These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following:

- 1) Enable the interrupt with the PIE bit;
- 2) Enable the SQW output pin with the SQWE bit;
- 3) Enable both at the same time and the same rate; or
- 4) Enable neither.

Table 3 lists the periodic interrupt rates and the square-wave frequencies that can be chosen with the RS bits. These four read/write bits are not affected by  $\overline{\text{RESET}}$ .



# Real-Time Clock

## Control Register B

MSB

LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

**Bit 7: SET.** When the SET bit is 0, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to 1, any update transfer is inhibited, and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit and is not affected by  $\overline{\text{RESET}}$  or internal functions of the device.

**Bit 6: Periodic Interrupt Enable (PIE).** The PIE bit is a read/write bit that allows the periodic interrupt flag (PF) bit in Register C to drive the  $\overline{\text{IRQ}}$  pin low. When the PIE bit is set to 1, periodic interrupts are generated by driving the  $\overline{\text{IRQ}}$  pin low at a rate specified by the RS3–RS0 bits of Register A. A 0 in the PIE bit blocks the  $\overline{\text{IRQ}}$  output from being driven by a periodic interrupt, but the PF bit is still set at the periodic rate. PIE is not modified by any internal device functions, but is cleared to 0 on  $\overline{\text{RESET}}$ .

**Bit 5: Alarm Interrupt Enable (AIE).** This bit is a read/write bit that, when set to 1, permits the alarm flag (AF) bit in Register C to assert  $\overline{\text{IRQ}}$ . An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes, including a don't-care alarm code of binary 11XXXXXX. The AF bit does not initiate the  $\overline{\text{IRQ}}$  signal when the AIE bit is set to 0. The internal functions of the device do not affect the AIE bit, but is cleared to 0 on  $\overline{\text{RESET}}$ .

**Bit 4: Update-Ended Interrupt Enable (UIE).** This bit is a read/write bit that enables the update-end flag (UF) bit in Register C to assert  $\overline{\text{IRQ}}$ . The  $\overline{\text{RESET}}$  pin going low or the SET bit going high clears the UIE bit.

The internal functions of the device do not affect the UIE bit, but is cleared to 0 on  $\overline{\text{RESET}}$ .

**Bit 3: Square-Wave Enable (SQWE).** When this bit is set to 1, a square-wave signal at the frequency set by the rate-selection bits RS3–RS0 is driven out on the SQW pin. When the SQWE bit is set to 0, the SQW pin is held low. SQWE is a read/write bit and is cleared by  $\overline{\text{RESET}}$ . SQWE is low if disabled, and is high impedance when  $V_{CC}$  is below  $V_{PF}$ . SQWE is cleared to 0 on  $\overline{\text{RESET}}$ .

**Bit 2: Data Mode (DM).** This bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions or  $\overline{\text{RESET}}$ . A 1 in DM signifies binary data, while a 0 in DM specifies BCD data.

**Bit 1: 24/12.** The 24/12 control bit establishes the format of the hours byte. A 1 indicates the 24-hour mode and a 0 indicates the 12-hour mode. This bit is read/write and is not affected by internal functions or  $\overline{\text{RESET}}$ .

**Bit 0: Daylight Saving Enable (DSE).** This bit is a read/write bit that enables two daylight saving adjustments when DSE is set to 1. On the first Sunday in April, the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM, it changes to 1:00:00 AM. When DSE is enabled, the internal logic test for the first/last Sunday condition at midnight. If the DSE bit is not set when the test occurs, the daylight saving function does not operate correctly. These adjustments do not occur when the DSE bit is 0. This bit is not affected by internal functions or  $\overline{\text{RESET}}$ .

# Real-Time Clock

## Control Register C

MSB

LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

**Bit 7: Interrupt Request Flag (IRQF).** This bit is set to 1 when any of the following are true:

PF = PIE = 1

AF = AIE = 1

UF = UIE = 1

Any time the IRQF bit is 1, the  $\overline{\text{IRQ}}$  pin is driven low. This bit can be cleared by reading Register C or with a  $\overline{\text{RESET}}$ .

**Bit 6: Periodic Interrupt Flag (PF).** This bit is read-only and is set to 1 when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to 1 independent of the state of the PIE bit. When both PF and PIE are 1s, the  $\overline{\text{IRQ}}$  signal is active and sets the IRQF bit. This bit can be cleared by reading Register C or with a  $\overline{\text{RESET}}$ .

**Bit 5: Alarm Interrupt Flag (AF).** A 1 in the AF bit indicates that the current time has matched the alarm time. If the AIE bit is also 1, the  $\overline{\text{IRQ}}$  pin goes low and a 1 appears in the IRQF bit. This bit can be cleared by reading Register C or with a  $\overline{\text{RESET}}$ .

**Bit 5: Update-Ended Interrupt Flag (UF).** This bit is set after each update cycle. When the UIE bit is set to 1, the 1 in UF causes the IRQF bit to be a 1, which asserts the  $\overline{\text{IRQ}}$  pin. This bit can be cleared by reading Register C or with a  $\overline{\text{RESET}}$ .

**Bits 3 to 0: Unused.** These bits are unused in Register C. These bits always read 0 and cannot be written.

## Control Register D

MSB

LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

**Bit 7: Valid RAM and Time (VRT).** This bit indicates the condition of the battery connected to the  $V_{\text{BAT}}$  pin. This bit is not writeable and should always be 1 when read. If a 0 is ever present, an exhausted internal lithium energy source is indicated and both the contents of

the RTC data and RAM data are questionable. This bit is unaffected by  $\overline{\text{RESET}}$ .

**Bits 6 to 0: Unused.** The remaining bits of Register D are not usable. They cannot be written and they always read 0.

DS12885/DS12887/DS12887A/DS12C887/DS12C887A



# Real-Time Clock

**Table 3. Periodic Interrupt Rate and Square-Wave Output Frequency**

SELECT BITS REGISTER A				t <sub>PI</sub> PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
RS3	RS2	RS1	RS0		
0	0	0	0	None	None
0	0	0	1	3.90625ms	256Hz
0	0	1	0	7.8125ms	128Hz
0	0	1	1	122.070μs	8.192kHz
0	1	0	0	244.141μs	4.096kHz
0	1	0	1	488.281μs	2.048kHz
0	1	1	0	976.5625μs	1.024kHz
0	1	1	1	1.953125ms	512Hz
1	0	0	0	3.90625ms	256Hz
1	0	0	1	7.8125ms	128Hz
1	0	1	0	15.625ms	64Hz
1	0	1	1	31.25ms	32Hz
1	1	0	0	62.5ms	16Hz
1	1	0	1	125ms	8Hz
1	1	1	0	250ms	4Hz
1	1	1	1	500ms	2Hz

### Update Cycle

The device executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to 1, the user copy of the double-buffered time, calendar, and alarm bytes is frozen and does not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers, and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corre-

sponding time byte and issues an alarm if a match or if a don't-care code is present in all three positions.

There are three methods that can handle RTC access that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle that indicates over 999ms is available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit pulses once per second. After the UIP bit goes high, the update transfer occurs 244μs later. If a low is read on the UIP bit, the user has at least 244μs before the time/calendar data is changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244μs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (Figure 3). Periodic interrupts that occur at a rate greater than t<sub>BUC</sub> allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within one (t<sub>PI</sub> + t<sub>BUC</sub>) to ensure that data is not read during the update cycle.

### Handling, PC Board Layout, and Assembly

The EDIP module can be successfully processed through conventional wave-soldering techniques so long as temperature exposure to the lithium energy source does not exceed +85°C. Post-solder cleaning with water-washing techniques is acceptable, provided that ultrasonic vibration is not used. Such cleaning can damage the crystal.

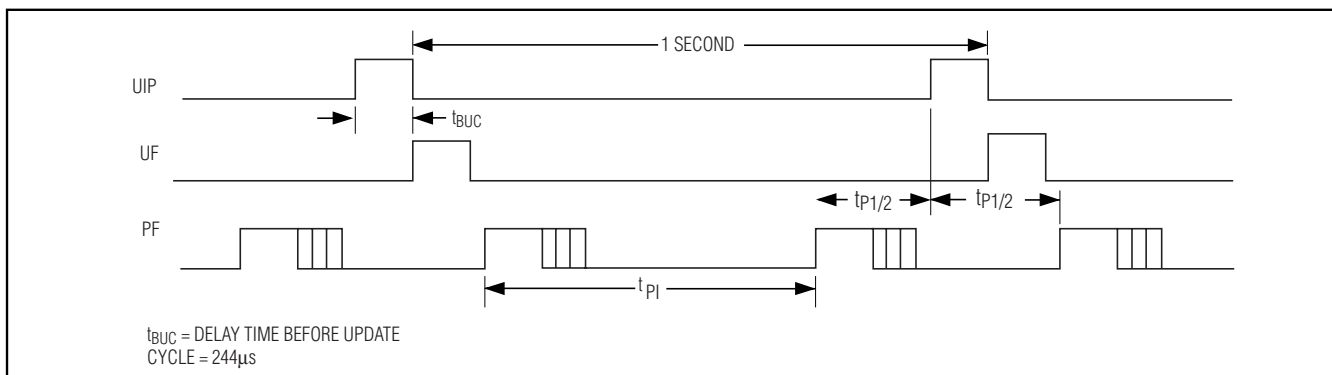
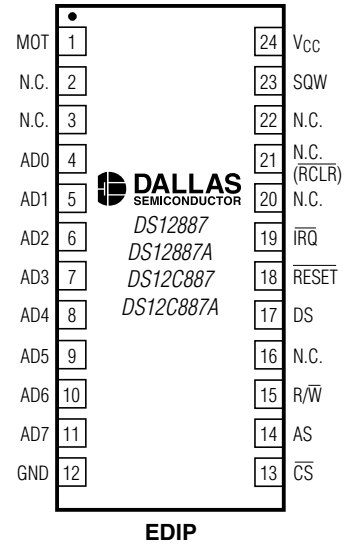
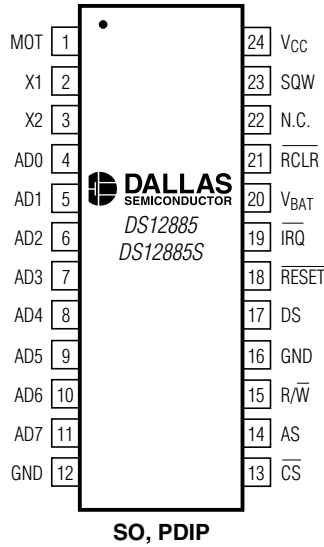


Figure 3. UIP and Periodic Interrupt Timing

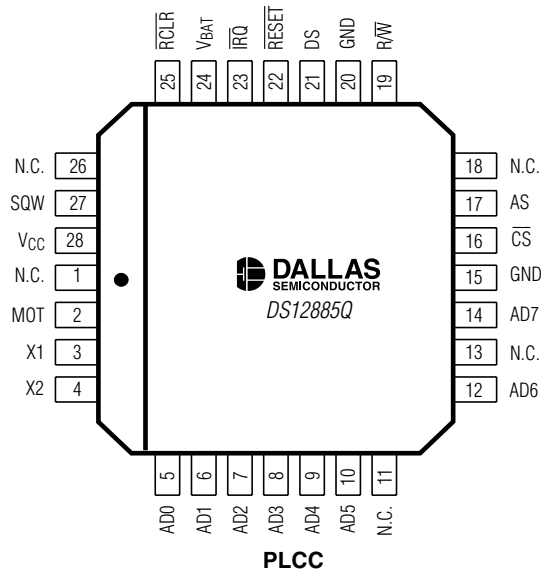
# Real-Time Clock

## Pin Configurations

TOP VIEW



( ) FOR THE DS12887A/DS12C887A.

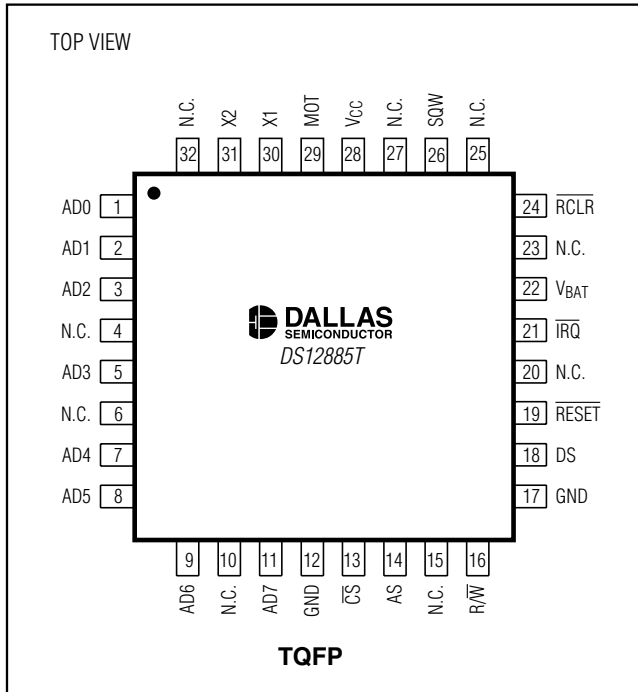


NOTE: THE DS12887A AND DS12C887A CANNOT BE STORED OR SHIPPED IN CONDUCTIVE MATERIAL THAT WILL GIVE A CONTINUITY PATH BETWEEN THE RAM CLEAR PIN AND GROUND.

# Real-Time Clock

DS12885/DS12887/DS12887A/DS12C887/DS12C887A

## Pin Configurations (continued)



## Thermal Information

PACKAGE	THETA-JA (°C/W)	THETA-JC (°C/W)
PDIP	75	30
SO	105	22
PLCC	95	25

## Package Information

PIN-PACKAGE	DOCUMENT NO.
24 SO (300 mils)	<b>56-G4009-001</b>
24 PDIP	<b>56-G5000-003</b>
24 EDIP	<b>56-G0001-001</b>
28 PLCC	<b>56-G4001-001</b>
32 TQFP	<b>56-G4004-001</b>

## Chip Information

TRANSISTOR COUNT: 17,000  
 PROCESS: CMOS  
 SUBSTRATE CONNECTED TO GROUND

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK*
<b>DS12885</b>	0°C to +70°C	24 PDIP	DS12885
DS12885+	0°C to +70°C	24 PDIP	DS12885
DS12885N	-40°C to +85°C	24 PDIP	DS12885
DS12885N+	-40°C to +85°C	24 PDIP	DS12885
DS12885Q	0°C to +70°C	28 PLCC	DS12885Q
DS12885Q+	0°C to +70°C	28 PLCC	DS12885Q
DS12885QN	-40°C to +85°C	28 PLCC	DS12885Q
DS12885QN+	-40°C to +85°C	28 PLCC	DS12885Q
DS12885Q/T&R	0°C to +70°C	28 PLCC	DS12885Q
DS12885Q+T&R	0°C to +70°C	28 PLCC	DS12885Q
DS12885QN/T&R	-40°C to +85°C	28 PLCC	DS12885Q
DS12885QN+T&R	-40°C to +85°C	28 PLCC	DS12885Q
DS12885S	0°C to +70°C	24 SO (300 mils)	DS12885S
DS12885S+	0°C to +70°C	24 SO (300 mils)	DS12885S
DS12885SN	-40°C to +85°C	24 SO (300 mils)	DS12885S
DS12885SN+	-40°C to +85°C	24 SO (300 mils)	DS12885S
DS12885S/T&R	0°C to +70°C	24 SO (300 mils)	DS12885S
DS12885S+T&R	0°C to +70°C	24 SO (300 mils)	DS12885S
DS12885T	0°C to +70°C	32 TQFP	DS12885
DS12885T+	0°C to +70°C	32 TQFP	DS12885
DS12885TN	-40°C to +85°C	32 TQFP	DS12885
DS12885TN+	-40°C to +85°C	32 TQFP	DS12885
DS12885T/T&R	0°C to +70°C	32 TQFP	DS12885
<b>DS12887</b>	0°C to +70°C	24 EDIP	DS12887
DS12887+	0°C to +70°C	24 EDIP	DS12887
DS12887A	0°C to +70°C	24 EDIP	DS12887A
DS12887A+	0°C to +70°C	24 EDIP	DS12887A
DS12C887	0°C to +70°C	24 EDIP	DS12C887
DS12C887+	0°C to +70°C	24 EDIP	DS12C887
DS12C887A	0°C to +70°C	24 EDIP	DS12C887A
DS12C887A+	0°C to +70°C	24 EDIP	DS12C887A

+ Denotes a lead-free/RoHS-compliant device.

T&R = Tape-and-reel.

\*A "+" anywhere on the top mark indicates a lead-free device, and an "N" indicates an industrial temperature range device.

# Real-Time Clock

## Revision History

- 
- Rev 0; 6/05: Initial release of combined data sheet.
  - Rev 1; 4/06: Corrected *Intel Bus Write Timing* diagram (page 4), *Intel Bus Read Timing*,  *$\overline{TRQ}$  Release Delay Timing*, and *Power-Up/Down Timing* diagrams (page 5), and *Functional Diagram* (page 7). Added *Handling*, *PC Board Layout*, and *Assembly* section (page 20).
  - Rev 2; 5/06: Corrected *Intel Bus Write Timing* diagram (page 4); added PLCC pin description information (pages 8, 9, and 10); changed pin 16 from N.C. to GND for the SO, PDIP packages (pages 8, 9, and 20).
  - Rev 3; 2/07: Corrected *Intel Bus Write Timing* diagram (page 4); updated Ordering Information (page 20); added Package Information table (page 20); removed package drawings (pages 22 to 27).

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