MEM8PLUS Version 2f Implementation Guide

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This document has several purposes with corresponding sections. First, a general overview of the features and options of the board - what it was designed to do and, sometimes, what it cannot do. Second is the Board Configuration section. Here is all the information for how to configure the board and its variety of options. The third main section is the front-panel operations section, where step-by-step instructions are provided for operating the front-panel option, including the program start feature.

Features Overview:

The MEM8PLUS has two distinct but interactive parts, which give it its name. MEM8 is a complete 8-bit memory implementation with static RAM up to 1MB, and EPROM or similar non-volatile memory up to 16K. This allocation was selected to be sufficient to run any 8-bit version of CP/M and was especially designed for banked CP/M3. With the full 1MB of RAM, there can be up to 16 banks of memory. By default, the board uses standard 16-bit addressing. An add-on option extends this to 24-bits for those CPUs with such capability. For the majority of 8-bit CPUs, there is an optional memory management unit to extend their addressing to the additional 15 banks provided on the board.

PLUS is the section of the board that gives it buss/system monitoring and front-panel features. This is totally optional and the MEM8 half of the board can be used without the PLUS options. PLUS can be indispensable for helping to bring up a new S-100 system, troubleshoot a malfunctioning system, help to test other S-100 boards, and as an aid to assembly language programming. Over the years, many S-100 systems were constructed without this capability, but it is believed that the general populace of current S-100 enthusiasts prefers systems with front panel capabilities.

Many of the capabilities of this board had their roots in the version 1 implementation, designed in 2006. Version 1 never made it past prototype, but several of the prototypes are still in use in running S-100 systems.

General Board Facts:

- Designed as a standard/compliant IEEE-696 S-100 8-bit slave.
- Requires only +8V. Current requirements vary between 0.5A and 2.3A, depending on options. Due to space and thermal considerations, only modern switching regulators were used in the design: the Pololu and SBC devices. Optionally, jumpers permit the board to operate directly on a 5V power supply with no regulators installed.
- All busses are fully buffered. Inputs from the bus have a standard LS-TTL load. Outputs to the bus should be capable of driving up to 20 properly buffered boards.
- S-100 bus pins 20, 53 and 70 have optional jumpers to Ground (0V).
- Board silk-screening should be adequate to convey the meaning of jumpers and switches. Additional information is on the schematics, and the board configuration section below.
- Unless specified, all board build options can be added to a functioning board at a later time to increase capabilities,

MEM8 (memory) details:

- All memory configuration, with but two exceptions explained below, is done with dip-switches.
- One 28-pin ROM socket will accept 5-volt only 2716 (2K), 2732 (4K), 2764 (8K) or 27128 (16K) type non-volatile memory such as ROM, EPROM or EEPROM.
- The ROM can start at any 4K address between 8000 and F000.
- ROM size is selectable as 2K, 4K, 8K or 16K. This permits the use of a small code set in a larger device without wasting memory space. (For example, a monitor that only needs 4K, but the device is actually an 8K device.)
- Without any options installed, the ROM space will typically overlay RAM.
- Two 32-pin sockets are provided for RAM. RAM chips can be 32K, 128K or 512K parts. The board will run with just one chip or both, so memory sizes of 32K, 64K, 128K, 256K, 512K and 1M are possible. (Note: mixed chip sizes have not been tested.)
- Without the battery-backed RAM option (described below), four jumpers are needed. They can be soldered wire jumpers or 2-pin headers with shorting shunts.

MEM8 options:

- A ROM Wait-State generator can provide from 1 to 8 wait-states for all ROM memory accesses to ensure reliable ROM operation for faster CPUs. The number of wait-states is set by jumpers.
- 24-bit capable CPUs, using the extended address bus, can directly address the whole 1MB of RAM on the board. The address decoder has switches to place the board anywhere in the 24-bit range. With this option, the memory of multiple boards can be used together.
- By utilizing very low-power RAM chips, and installing the memory power controller ICs and on-board batteries, this board can retain the contents of RAM when the power is turned off. (This feature was present in version 1 and RAM contents have been retained for several years.) When this option is installed, the 4 jumpers described in the MEM8 details above must be removed.
- A Memory Manager can provide access to as many as 16 64K banks of memory, depending on how much actual RAM is installed and the mode of operation. This is implemented as a 4-bit output port that can switch up to 4 banks of memory in normal “Cromemco” mode. The address of the output port can be any 8-bit address. In the Cromemco mode, a single bit in the port is raised to activate a bank. Also valid is the state when no bits are raised, as is the case after reset and before the CPU selects any banks. When the CPU makes a bank selection, only one bit can be active at a time, hence the four-bank limit. The same four bits can address the full 16 banks if configured in encoded mode where multiple high bits are allowed. Thus, 1010, invalid in Cromemco mode, would activate bank 9 in encoded mode. The MMU can operate with dip-switch-selectable memory common sizes of 8K, 16K, 24K or 32K, providing flexibility for OS configuration. Due to the nature of the MMU operation, it can only address on-board memory and use of a MEM8PLUS board with this option is mutually exclusive with the 24-bit address option and the use of multiple boards on the same bus.
- The MMU active bank option adds a display to the MMU. With this, one may observe which bank is currently active by means of four discrete LEDs or a hexadecimal display. Note that this option requires the System Monitor option described in the PLUS details below.

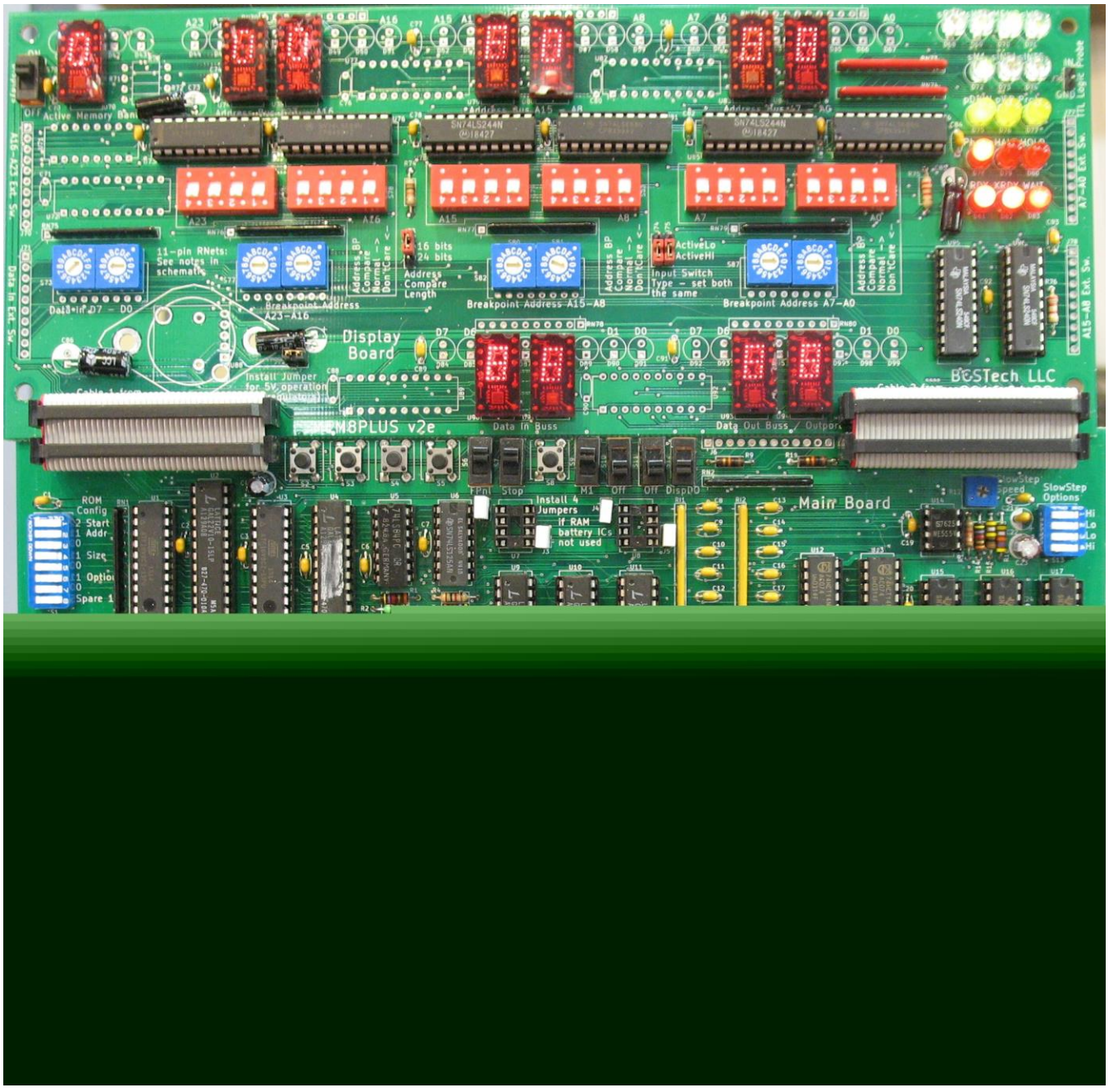
PLUS details:

All PLUS features are options and can be added to the MEM8 at initial build, or later as the user/operator desires.

- System Monitor Option: This is the base of the PLUS features. No other PLUS options are possible without this.
  When fabricated, the MEM8PLUS board is actually two boards that are initially attached to each other. First is the 10" by 6" S-100 Main Board. (Yes, 6 x 10 is one inch higher than the standard, but it is still within the IEEE-696 specification, and the extra inch provides space for some front panel components that need to be accessible when the board is plugged in.) This contains all the components to operate the MEM8 part of the design, plus many of the parts of the PLUS section. Then, on top of the Main board is a 10" by 4" board called the Display Board. The two may be used as-is, or, for certain physical configurations, like bringing the displays on the display board to a front panel, they may be snapped apart and then connected together with two inexpensive 40-pin ribbon cables.
  The display board, in its minimum configuration as a systems monitor board, has 16 LEDs or four hexadecimal displays to show the contents of the Address bus, 8 LEDs or two hexadecimal displays to show the contents of the Data Input bus, 8 LEDs or two hexadecimal displays to show the contents of the Data Output bus, and 15 LEDs to show the important status and control signals on the bus. A switch on the board turns the displays ON or OFF.
- Extended Address System Monitor Option: This adds 8 LEDs or two hexadecimal displays to show the contents of the extended address bus, A16 to A23. This option would be useful when the 24-bit memory option (described above) is selected, or the Memory Management option is installed.
- Logic Probe Option: A simple TTL logic probe is provided. It reads only TTL levels and displays on a single LED.
- Front-panel Operations Option: This option extends the System Monitor Option to a fully-functional front panel. All these features are enabled by this option:
  - Hardware CPU Stop and Start. A switch, when set to STOP will stop the running CPU on the next machine (M) cycle. When set to RUN, the CPU will start running again at full speed.
  - A momentary pushbutton switch will step the CPU one M cycle when the CPU is stopped.
  - Single-Step by M1 or any M cycle switch. When this switch is set to M1 stepping mode, and the Step switch is pressed, the CPU will be permitted to run until the next M1 cycle where it will stop. In the any M cycle stepping mode, the CPU will stop in the next M cycle, regardless of status. This can be used to view non-M1 memory read, memory write, Input and Output port operations and Interrupt Acknowledge cycles.
  - Full or variable speed slow-step selected by switch. When set to full-speed, the CPU runs at full clock speed. When set to variable speed, the CPU will automatically step at a user-selectable rate from as low as about one cycle every 5 seconds, up to several hundred cycles per second.
  - Hardware 16 bit address breakpoint with enable/disable. A switch controls this feature. When set to disable, no hardware breakpoints are triggered. When set to enabled, the hardware will stop the CPU when the address set in the breakpoint switches is encountered. This feature will break regardless of the location of the code: any on-board RAM or ROM. There are several sub-options:

        - 24-bit address breakpoint is a build option. When installed, a jumper permits selection of either 16-bit or 24-bit operation.
        - Three switch options are available during build for setting the breakpoint address (one must be selected):
            - Standard 8-position DIP switch.
            - Rotary hexadecimal switch. These make setting addresses very easy. They come in active high and active low versions. Either can be used. Different pull-up/pull-down resistors are required and two jumpers must change between the two options. Details are in the schematics and the construction notes.
            - External via headers. The user can use any available or desirable SPST switches. They can be wired in either active-high or active low (but all must be the same), and like the rotary hex switches, there are resistor and jumper considerations.
        - Range switches - these switches will enable setting an address range for the breakpoint. This is done by permitting each and every bit (16 or 24) to be designated as "don't care". For example, if a 16-bit breakpoint is set to F663, and the two least significant bits are set to "don't care", then a break will occur on F660, F661, F662 or F663.
    - An 8-bit output "test" port that can be written by the CPU and displayed on the data out bus display. It can be addressed at any 8-bit I/O port. A switch is used to select if the output port or the data out bus shows on the display.
    - An 8-bit input "test" port that reads a set of 8-bit data input switches on the display board. It uses the same port address as the output test port. The data input switches have the same dip-switch, hex rotary or off-board options as the breakpoint address switches discussed above.
    - Memory Examine, Memory Examine Next, Deposit and Deposit Next pushbutton switches are provided to enable low-level memory operations when the CPU is stopped. These switches are available to the user when the Front Panel enable switch is moved from Normal to Front Panel. These functions operate directly with the on-board memory. The breakpoint set switches double as memory address switches for these functions, and data for the deposit operations are taken from the 8-bit data input switches described previously in the "test" input port feature.
    - All front-panel control switches are self-contained and easily accessible at the top edge of the main board using miniature tactile push-button switches and miniature slide switches. Optionally, they can be duplicated on an external control pod or with switches mounted on the front of an enclosure. A header is provided for this possibility.
    - For 8080, 8085 and Z80 processors only, a program run function is provided that can force the CPU to any location in memory and have it begin execution there. Existing switches are double-purposed to allow the operator to set a 16-bit start address, and optionally, a memory bank. Then the program can be started at that address in stopped, slow-stepped or full-speed execution modes. Along with the memory examine and deposit functions, complete programs can be "toggled" into the computer at any memory address and run from there, even without a terminal of any kind or a monitor program ROM.

A picture is worth a thousand words:



Mem8Plus board shown with the Display Board seperated from the Main Board, and then re-connected with two very short ribbon cables. This board is configured to run on a 5V bus (no regulators). It has all options installed except the battery-backed RAM, the Extended 24-bit addressing and the external switch options. As shown, it has a 2K 2716 monitor in ROM running at F000H and two 32K RAM chips. The board will boot and run CP/M 2.2, and it is expected to run banked CP/M 3 with the memory increased to at least 128K. The bank select port is configured to 40H; the Test I/O port is set to FFH.

Currently, there are no patches on the board. However, the battery-backed RAM option is unavailable due to a design flaw that cannot be patched easily.

Mem8Plus Board Configuration:

This section describes the function of the jumpers and dip switches for proper configuration of the board and its many options. Note that these descriptions are without regard to the actual installed options and some may not be applicable.

Power Configuration:

J11, Main board - Mutually exclusive with the on-board voltage regulator options, this jumper is connected (shorted with a shorting shunt) to provide 5V power from a bus designed for 5 volt operation.

J72, Display board - Mutually exclusive with the on-board voltage regulator options, this jumper is connected (shorted with a shorting shunt) to provide 5V power from a bus designed for 5 volt operation.

J13, J14 and J15, Main board - Provides additional system ground pins on the bus. If the system this board is going into provides these additional ground pins on pin 20, 53 and 70, short the appropriate jumper to take advantage of this bus feature.

ROM Wait States:

J10, Main board. With no jumpers installed, the ROM Wait-State feature is disabled. To enable one wait-state, jumper the two pins labeled "1". For two wait states, jumper "1" and "2". Select up to 8 wait states by adding additional jumpers. Don't remove previously installed jumpers.

Extended 24-bit address board select:

J8, Main board. Insert shorting jumpers to select the board address from one of 16 possible start locations in the 24-bit S-100 extended address space (16MB). The chart here shows all the possibilities:

Board Address	A23	A22	A21	A20
0xxxx	ON	ON	ON	ON
1xxxx	ON	ON	ON	OFF
2xxxx	ON	ON	OFF	ON
3xxxx	ON	ON	OFF	OFF
4xxxx	ON	OFF	ON	ON
5xxxx	ON	OFF	ON	OFF
6xxxx	ON	OFF	OFF	ON
7xxxx	ON	OFF	OFF	OFF
8xxxx	OFF	ON	ON	ON
9xxxx	OFF	ON	ON	OFF
Axxxx	OFF	ON	OFF	ON
Bxxxx	OFF	ON	OFF	OFF
Cxxxx	OFF	OFF	ON	ON
Dxxxx	OFF	OFF	ON	OFF
Exxxx	OFF	OFF	OFF	ON
Fxxxx	OFF	OFF	OFF	OFF

Battery-backed RAM:

J2, J3, J4 & J5, Main board. Insert these jumpers when the battery-backed RAM option is not installed. If battery-backed RAM is installed, U7 and U8 will be present, and one or two 2032 coin cells will be inserted into battery clips BT1 and BT2 at the lower right corner of the board.

MMU/Bank Select Port Address Configuration:

J9, Main board.
Use this set of configuration jumpers to select the I/O port that the Bank Select Register will respond to. Any 8-bit address may be selected by jumping adjacent pins with shorting shunts. A shunt on the pins selects that bit to be a zero. Off is a one.

Test I/O Port Address Configuration:

J12, Main board.
Use this set of configuration jumpers to select the I/O port of the test register. Any 8-bit address may be selected by jumping adjacent pins with shorting shunts. A shunt on the pins selects that bit to be a zero. Off is a one. The test register consists of a simple 8-bit input port and a simple 8-bit output port. When read from, the input port responds with the byte set on the Data In switches (S73 - binary, or S71 & S72 - hex). When written to, the byte output is displayed on the Outport display (shared with the Data out Bus) if the S12 is set to DispTP.

ROM Configuration Dip-Switch:

S2, Main board.
The first three positions, Labeled Start Addr 2, 1 and 0, control the starting address of the ROM socket within the standard 16-bit address space. Off, Open and 1 are typical nomenclatures used on dip switches. This table shows the addressing possibilities:

Start Address	Sw2	Sw1	Sw0
8000H	On	On	On
9000H	On	On	Off
A000H	On	Off	On
B000H	On	Off	Off
C000H	Off	On	On
D000H	Off	On	Off
E000H	Off	Off	On
F000H	Off	Off	Off

Positions 4 and 5: Labeled Size 1 and 0 - these are set to correspond to the size of the memory device in the ROM socket. Not only do they set the proper logic, but they also configure the socket pins that change between the various sized devices.

Size (typical device)	Sw1	Sw0
2K (2716)	On	On
4K (2732)	On	Off
8K (2764)	Off	On
16K (27128)	Off	Off

Positions 6 and 7: Labeled Option 1 and 0 are used to set one of several operating modes of the ROM logic as described in the table below. Note that these options also depend on the EAddrOn (M24) switch on the RAM/MMU Config dip switch.

Option 1	Option 0	24-bit On	Function
On	On	Don't Care	ROM disabled
On	Off	Yes	ROM Enabled in lowest 64K
Off	On	Yes	ROM Enabled in highest 64K
Off	Off	Yes	ROM disabled
On	Off	No	ROM Enabled in "ROM Bank" only
Off	On	No	ROM Enabled in "ROM Bank" & lowest MMU bank
Off	Off	No	ROM Enabled in "ROM Bank" & highest MMU bank

The "ROM bank" referred to in the table above is the name for the state the MMU logic is in just after reset and before the CPU writes anything to the MMU Bank Select Port. In this state, the lowest 64K of RAM is enabled and the ROM overlays RAM as set by the ROM size and start address switches. Once the CPU writes anything to the Bank Select Port, the ROM Bank disappears.

Position 8 is unused, labeled Spare 1.

RAM/MMU Configuration Dip-Switch:

S14, Main board.
Positions 1 and 2 select the RAM chip size. The table shows all options:

Size	Sw1	Sw0
RAM Disabled	On	On
32K	Off	Off
128K	On	Off
512K	Off	On

Position 3 switches the board between 24-bit extended addressing and enabling the MMU. They cannot be both enabled at the same time. Off for 24-bit, On to enable the MMU if installed.

Position 4 is the ROM option switch. This switch is used only when 24-bit extended addressing is enabled and defines the location of the ROM. If set to On, the ROM will appear at x0xxxxH in the 24-bit address space. If set to Off, the ROM will appear at FxxxxH in the 24-bit address space. The ROM's location within the 64K page is configured with the ROM dipswitch.

Positions 5 and 6 - MMU Common Size. To afford as much flexibility as possible, the board was designed with four possible memory common sizes. The correct selection will depend on the OS.

Size	Sw1	Sw0
8K	On	On
16K	On	Off
24K	Off	On
32K	Off	Off

Position 7 determines the bank select mode of the MMU: Normal Cromemco style bank select or Encoded bank select. With the switch On, normal mode is selected and up to four banks can be selected by writing a '1' bit to the position in the bank select register corresponding to the desired bank. For example, writing a 04H (0000 0100) will select bank 4. Only one bit may be high at any one time, and only the lowest four bits are used, limiting this mode to just four selectable banks. Encoded mode works by permitting any combination of the lowest four bits to be high. Thus, there are 16 possible combinations that can select up to 16 banks of RAM, the maximum the board can contain.
Note; the bank display is designed for encoded mode, to show all 16 banks. In Cromemco mode, the display is a subset of encoded mode, just the single high bit patterns.

Display	Actual Bank
0	0 (ROM Bank)
1	1
2	2
4	3
8	4

Position 8 is unused, labeled Spare 2.

Slow-Step Configuration Dip-Switch:

S13, Main board.
This dip switch selects various combinations of resistors and capacitors for the slow-step oscillator in order to provide a wide range of automatic stepping speeds. Due to component tolerances, the oscillator frequency is best determined empirically. That is, try all the combinations of capacitors and resistors; they interact with each other. Also, note that the Slow Step Speed control R12 provides a means of continuously varying the speed to get just the speed needed.

Switch	Label	Setting	Function/operation
1	RHi	On	100K timing resistor not selected - higher frequencies
1	RHi	Off	100K timing resistor selected - lower frequencies
2	RLo	On	47K timing resistor not selected - higher frequencies
2	RLo	Off	47K timing resistor selected - lower frequencies
3	CLo	On	0.47μF timing capacitor selected - lower frequencies
3	CLo	Off	0.47μF timing capacitor not selected - higher frequencies
4	CHi	On	4.7μF timing capacitor selected - lower frequencies
4	CHi	Off	4.7μF timing capacitor not selected - higher frequencies

Address Compare Length:

J73, Display board.
This jumper selects the breakpoint address compare length. If the 24-bit Breakpoint Address option is not installed, or the operator wishes to ignore the upper 8 bits (A16 to A23) and monitor only A0 to A15, this jumper will be set to 16 bits. For full 24-bit breakpoint monitoring, set the jumper to 24 bits.

Input Switch Type:

J74 & J75, Display board.
These two side-by-side jumpers are ALWAYS set the same. Along with the pull-up/pull-down resistors on the dip or rotary hex switches, they help accommodate both active-high and active-low switches. By their very nature, dip switches are either active-high or active- low depending on how they are wired. However, they work best in the active-low mode as used on this board. Hex rotary switches can be either active high or active-low, depending on the manufacturer. (And one brand, at least, makes a unit that is both.) When the board is constructed (see construction notes), decisions are made on how to populate the resistors and these two jumpers. Once built, there should not be a need to change these jumpers.

Front Panel Operations:

This section will help the user become familiar with the operation of the front-panel features.

To have a base point for discussion, ensure the switches are set as such:

S6 - Normal/FPnl in Normal
S7 - Run/Stop in Run
S9 - Any/M1 in M1
S10 - SlwStp/Off in Off
S11 - BPOn/Off in Off
S12 - DispTP/DispDO in DispDO

Also, it is assumed that the computer is running a program of some kind, such as a basic ROM monitor or an operating system such as CP/M.

- To stop a running CPU, move the Run/Stop switch (S7) to Stop.
- To start a stopped CPU, move the Run/Stop switch (S7) to Run.
- To single-step the CPU, first stop it. Then press the Step button. Stepping will be by M1 cycle or any M cycle depending on the setting of S9 - Any or M1.
- To automatically slow-step the CPU, first stop it. Then move S10 to SlwStp. Stepping will occur at a rate determined by the slow-step oscillator.
- To change the slow-step rate, adjust the Slow Step Speed control R12. The speed is also controlled by various combinations of the switches in S13. See the section above relating to the configuration of the slow-step dip-switch for more details.

- To program a specific hardware breakpoint, set the desired break address on the dip or hex Breakpoint Address switches on the display board. Ensure that all Address BP Compare range switches are set to Normal. Then move S11 to BPOn. When a running program encounters the address set on the switches, the CPU will be stopped on that address.

- To resume running the program after a breakpoint, move the Run/Stop switch to Stop, then move the BPOn/Off switch to Off, then move the Run/Stop switch to Run.

- To program a range of addresses for hardware breakpoint, first set the lowest address of the range on the breakpoint address switches. Then move as many of the range switches as are necessary to include all addresses needed in the range. For example, suppose a break range is needed from 8660H to 8663H. Set 8660H into the Breakpoint Address switches, then set the A0 and A1 BP Compare switches to don't care. The lowest two bits of the address will be ignored and a break will occur when any of the addresses in the range are encountered after setting the BPOn/Off switch to BPOn.

- To display the output of the test output port, move the DispTP/DispDO (S12) switch to DispTP. Move it back to see the Data Out bus again.

- To examine (view) the contents of a memory address, first Stop the CPU and then move the Normal/FPnl switch (S6) to FPnl. Next set the address to examine into the Breakpoint Address switches. Then press the MemEx button (S2). The contents of memory at the chosen address will show on the data display.

- To increment and display the contents of the next memory address after examining one, press the MemExNxt button (S3) The memory address will increment and show those contents on the data display.

- To deposit (write) a new byte into a memory address, first use MemEx and/or MemExNxt to arrive at the memory address desired. Next set the byte on the Data In switches. Then press the Deposit button. The data will be written to memory and show on the display.

- To quickly write several bytes in sequence, use MemEx and/or MemExNxt to arrive at the desired address. Next set the byte on the Data In switches. Then press the DepNxt button. The data will be written and the address will automatically be incremented, ready for entering another byte. Note that the byte written will not appear, but instead the contents of the next memory location will show on the data display.

- To use the program start feature with an 8080, 8085 or Z80 CPU, first note that the MemEx, MemExNxt, Deposit and DepNxt buttons are re-purposed. Unfortunately, there was not the room on the board to put this nomenclature. This feature works by jamming a three-byte Jump opcode and start address onto the CPU bus and cycle-stepping the CPU to read these bytes. This operation takes several steps:

    a. Be sure the CPU is stopped.
    b. Optionally, enter the bank number of the location of the desired start address on the Data Input switches and press the MemEx (Set Bank) button. If the bank display option is available, the bank will show on the display. If the MMU option is installed, A16 - A23 may also change based on MMU configuration and physical address.

c. Set the high half of the start address on the Data Input switches and press the MemExNxt (Set high address) button. The A16 - A23 address may change depending on the MMU configuration and the physical address.
d. Set the low half of the start address on the Data Input switches and press the Deposit (Set low address) button. The A16 - A23 address may change depending on the MMU configuration and the physical address.
e. Move the Step Type switch (S9) to Any.
f. Press the DepNxt (Load) button and observe hex C3 (binary 1100 0011) on the data display.
g. Press the Step button (S8). Notice that the address display increments, although this is irrelevant. The CPU's address is being ignored.
h. Press the DepNxt (Load) button again and see the low half of the start address in the data display.
i. Press the Step button again. The address display again increments with no effect.
j. Press the DepNxt (Load) button again and see the high half of the start address on the data display.
k. Press the Step button again.
l. Press the DepNxt button a fourth time to end the Load sequence. Observe the complete start address now showing on the address display, and the byte of code to be executed next from memory addressed by the CPU in the data display.
m. At this point, the CPU has been faked into executing a Jump instruction to the desired start address and the logic is in a normal stopped CPU state. From here it can be stepped (press the step button), slow-stepped (switch Slow-step on) or executed at full speed (move the Run/Stop switch to Run.)

End of Mem8Plus Implementation Guide.

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