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;PALASM Design Description

;---------------------------------- Declaration Segment ------------
TITLE    Ports selection for ISA adaptor for VGA bords.
PATTERN  Non Latched
REVISION 0
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COMPANY
DATE     03/29/14

CHIP VGA_IO  PALCE22V10                          ; Device not selected

;---------------------------------- PIN Declarations ---------------

PIN 1   bpSYNC                                  ;S100 bus address valid when high
PIN 2   bsVAL                                   ;S100 bus address valid when low
PIN 3   SA0                                     ;ISA Address line 0
PIN 4   SA1                                     ;ISA Address line 1
PIN 5   SA2                                     ;ISA Address line 2
PIN 6   SA3                                     ;ISA Address line 3
PIN 7   SA4                                     ;ISA Address line 4
PIN 8   SA5                                     ;ISA Address line 5
PIN 9   SA6                                     ;ISA Address line 6
PIN 10  SA7                                     ;ISA Address line 7
PIN 11  bsOUT                                   ;S100 Port Output

PIN 13  bsINP                                   ;S100 Port Input
Pin 14  bsINTA                                  ;S100 INTA
Pin 15  VGA_PORTS                               ;VGA Port selected* (OUTPUT LOW)
Pin 16  SA8                                     ;ISA Address line 8
Pin 17  SA9                                     ;ISA Address line 9
Pin 18  SA10                                    ;ISA Address line 10
Pin 19  SA11                                    ;ISA Address line 11
Pin 20  SA12                                    ;ISA Address line 12
Pin 21  SA13                                    ;ISA Address line 13
Pin 22  SA14                                    ;ISA Address line 14
Pin 23  SA15                                    ;ISA Address line 15


;---------------------------------- Boolean Equation Segment ------

EQUATIONS

/VGA_PORTS    =      /SA15 * /SA14 * /SA13 * /SA12 * /SA11 * /SA10 * /SA9 * SA8         ;Port 102H,103H OUT
                   * /SA7 * /SA6 * /SA5 * /SA4 * /SA3 * /SA2 * SA1
                   * bsOUT * /bsINTA

                 +   /SA15 * /SA14 * /SA13 * /SA12 * /SA11 * /SA10 * /SA9 * SA8         ;Port 102H,,103H IN
                   * /SA7 * /SA6 * /SA5 * /SA4 * /SA3 * /SA2 * SA1
                   * bsINP * /bsINTA

                +   /SA15 * /SA14 * /SA13 * /SA12 * /SA11 * /SA10 * SA9 * SA8          ;Port 03BxH OUT
                    * SA7 * /SA6 * SA5 * SA4
                    * bsOUT * /bsINTA

                 +   /SA15 * /SA14 * /SA13 * /SA12 * /SA11 * /SA10 * SA9 * SA8         ;Port 03BxH IN
                    * SA7 * /SA6 * SA5 * SA4
                    * bsINP * /bsINTA

                 +   /SA15 * /SA14 * /SA13 * /SA12 * /SA11 * /SA10 * SA9 * SA8          ;Port 03CxH  - 03DXH OUT
                    * SA7 * SA6 * /SA5
                    * bsOUT * /bsINTA

                 +   /SA15 * /SA14 * /SA13 * /SA12 * /SA11 * /SA10 * SA9 * SA8          ;Port 03CxH  - 03DXH IN
                    * SA7 * SA6 * /SA5
                    * bsINP * /bsINTA
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                +   /SA15 * SA14 * /SA13 * /SA12 * /SA11 * SA10 * SA9 * /SA8          ;Port 46E8H,4689H IN
                    * SA7 * SA6 * SA5 * /SA4 * SA3 * /SA2 * /SA1
                    * bsINP * /bsINTA

                +   /SA15 * SA14 * /SA13 * /SA12 * /SA11 * SA10 * SA9 * /SA8          ;Port 46E8H,4689H OUT
                    * SA7 * SA6 * SA5 * /SA4 * SA3 * /SA2 * /SA1
                    * bsOUT * /bsINTA


                +   /SA15 * /SA14 * /SA13 * /SA12 * /SA11 * /SA10 * /SA9 * /SA8        ;Port 80H, 81H OUT (AT
Diagnostic Port)
                    * SA7 * /SA6 * /SA5 * /SA4 * /SA3 * /SA2 * /SA1
                    * bsOUT * /bsINTA



          ;        +   /VGA_PORTS * bpSYNC * /bsVAL                                  ;Latch data
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