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TITLE    ISA BusCORE MEM & IO R/W Signals
PATTERN
REVISION 2
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COMPANY
DATE     12/1/14

CHIP ISA_RW  PALCE22V10                        ; Device not selected

;---------------------------------- PIN Declarations ---------------

                                               ;----- INPUT SIGNALS -------
PIN 1   bpSYNC                                 ;Not used below
PIN 2   DUAL                                   ;High if back to back 8 bit bytes required
PIN 3   RD16_OE                                ;S100 bus 16  bit write (Active LOW)
PIN 4   WR16_OE                                ;S100 bus 16 bit read   (Active low)
PIN 5   IO_READY                               ;<--- LOW, ISA bus wait request
PIN 6   RAW_A0                                 ;S100 bus A0
PIN 7   ISA_SEL                                ;ISA board select
PIN 8   SHIFT1                                 ;Output from counter U20
PIN 9   SHIFT2                                 ;Output from counter U20
PIN 10  SHIFT3                                 ;Output from counter U20
PIN 11  SHIFT4                                 ;Output from counter U20
PIN 13  SHIFT5                                 ;Output from counter U20
PIN 14  SHIFT6                                 ;Output from counter U20
PIN 15  SHIFT7                                 ;Output from counter U20
PIN 16  SHIFT8                                 ;Output from counter U20

                                               ;----- OUTPUT SIGNALS --------

PIN 17  STOP_CLOCK                             ;Stop clock PHI signal on U20
PIN 18  GAL_XRDY                               ;<--- LOW,  ISA wait request to S100 bus
PIN 19  GAL_A0                                 ;ISA A0
PIN 20  W_LOW                                  ;ISA memory low byte write
PIN 21  W_HIGH                                 ;ISA memory high byte write
PIN 22  R_LOW                                  ;ISA memory low byte read
pin 23  R_HIGH                                 ;ISA memory high byte read.

;---------------------------------- Boolean Equation Segment ------

EQUATIONS

/R_LOW          =       SHIFT2 * /SHIFT3  *  /RD16_OE * DUAL
/W_LOW          =       SHIFT2 * /SHIFT3  *  /WR16_OE * DUAL

GAL_A0          =       ISA_SEL * RAW_A0  * /DUAL
                      + SHIFT4  * DUAL

/R_HIGH         =       SHIFT5  * /SHIFT6  *  /RD16_OE  * DUAL
/W_HIGH         =       SHIFT5  * /SHIFT7  *  /WR16_OE  * DUAL


/GAL_XRDY       =       ISA_SEL * /IO_READY         ;Hold CPU if ISA board wants more time

STOP_CLOCK      =       ISA_SEL * IO_READY * DUAL   ;ALSO stop further shifts until ISA is ready
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