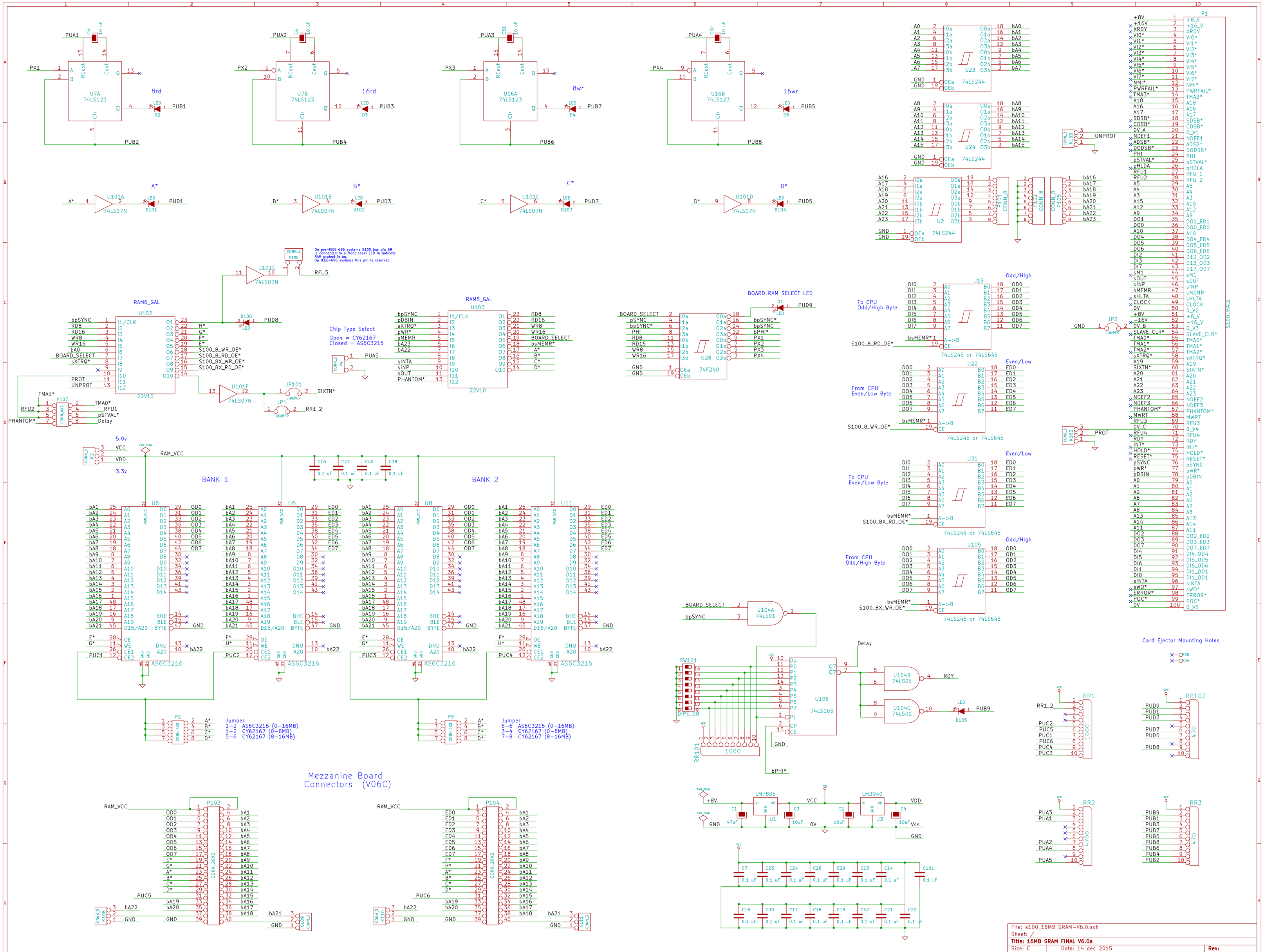
U7A 74LS123
U7B 74LS123
U16A 74LS123
U16B 74LS123
8rd
16rd
8wr
16wr
U101A 74LS07N
U101B 74LS07N
U101C 74LS07N
U101D 74LS07N
U101E 74LS07N
U101F 74LS07N
U23 74LS244
U24 74LS244
U2 74LS244
U19
U22
U31
U105
74LS245 or 74LS645
U28 74F240
U104A 74LS01
U104B 74LS01
U104C 74LS01
U106 74LS165
SW101 DIP5_08
RR101 1000
RR1 1000
RR102 470
RR2 4700
RR3 470
RAM6_GAL U102 22V10
RAM5_GAL U103 22V10
On pre-IEEE 696 systems S100 bus pin 69 is connected to a front panel LED to indicate RAM protect is on.
On IEEE-696 systems this pin is reserved.
Chip Type Select
Open = CY62167
Closed = AS6C3216
BOARD RAM SELECT LED
Odd/High
Even/Low
To CPU Odd/High Byte
From CPU Even/Low Byte
To CPU Even/Low Byte
From CPU Odd/High Byte
Card Ejector Mounting Holes
BANK 1
BANK 2
U5 AS6C3216
U6 AS6C3216
U8 AS6C3216
U11 AS6C3216
Jumper
1-2 AS6C3216 (0-16MB)
1-2 CY62167 (0-8MB)
5-6 CY62167 (8-16MB)
3-4 CY62167 (0-8MB)
7-8 CY62167 (8-16MB)
Mezzanine Board Connectors (V06C)
P103 CONN_20X2
P104 CONN_20X2
LM7805 U1
LM3940 U3
P1 S100_MALE
File: s100_16MB SRAM-V6.0.sch
Sheet: /
Title: 16MB SRAM FINAL V6.0a
Size: C
Date: 14 dec 2015
Rev:
KiCad E.D.A. eeschema (2013-07-07 BZR 4022)-stable
Id: 1/1