CBIOS as described in the Alteration Guide. Once done, and you like the way your 16K system operates, use MOVCPM to generate a system compatible with your memory size, reassemble your CBIOS for that memory size, reassemble your boot on Track 0 Sector 1 for your memory size and link them together using DDT.

```
0010 =       MEMSIZE EQU     16
2880 =       CPMBASE EQU     MEMSIZE*1024-1780H
3E00 =       LOCN    EQU     MEMSIZE*1024-2*256
3106 =       BDOS    EQU     (MEMSIZE-8)*1024+1106H
3E00                 ORG     LOCN

                     JUMP TABLE ENTRY

3E00 C3463E          JMP     BOOT
             WBOOTE:
3E03 C3733E          JMP     WBOOT
3E06 C3053F          JMP     CONST
3E09 C3ØD3F          JMP     CONIN
3E0C C31E3F          JMP     CONOUT
3E0F C32C3F          JMP     LIST
3E12 C31E3F          JMP     PUNCH
3E15 C30D3F          JMP     READER
3E18 C303C0          JMP     HOME
3E1B C306C0          JMP     SELDSK
3E1E C309C0          JMP     SETTRK
3E21 C30CC0          JMP     SETSEC
3E24 C30FC0          JMP     SETDMA
3E27 C312C0          JMP     READ
3E2A C315C0          JMP     WRITE

             SIGNON:
3E2D 0D0A0A          DB      CR,LF,LF
3E30 3136            DB      MEMSIZE/10+'0',MEMSIZE MOD 10 + '0'
3E32 4B20            DB      'K WMC CP/M'
3E3C 2056455253      DB      ' VERS 1.4'
3E45 00              DB      0

             BOOT:
3E46 318000          LXI     SP,0080H
3E49 3E04            MUI     A,04H           ;INITIALIZE 3P+S
3E4B D300            OUT     0
3E4D 212D3E          LXI     H,SIGNON
3E50 CDFA3E          CALL    PMSG
3E53 3E02            MUI     A,2
3E55 D384            OUT     84H             ;SELECT B DRIVE FOR TEST
3E57 DB80            IN      COMM
3E59 E680            ANI     80H
3E5B C2663E          JNZ     NOBEE
3E5E 3E01            MUI     A,1
3E60 320400          STA     DISKT
3E63 CD03C0          CALL    HOME
3E66 AF      NOBEE   XRA     A
3E67 320400          STA     DISKT
3E6A 324200          STA     0042H
3E6D CD03C0          CALL    HOME
```

```
3E70 C39E3E          JMP     GOCPM
                     ;
                     WBOOT:
3E73 318000          LXI     SP,0080H
3E76 3A0400          LDA     DISKT
3E79 3C              INR     A
3E7A D384            OUT     84H
3E7C CD03CO          CALL    HOME
3E7F 0E01            MVI     C,1
3E81 CDOCCO          CALL    SETSEC
3E84 018028          LXI     B,CPMBASE
3E87 CDOFCO          CALL    SETDMA
3E8A CDCC3E          CALL    MULTREAD
3E8D OE01    READ1:  MVI     C,1
3E8F CD09CO          CALL    SETTRK
3E92 CDOCCO          CALL    SETSEC
3E95 018035          LXI     B,CPMBASE+26*128
3E98 CDOFCO          CALL    SETDMA
3E9B CDCC3E          CALL    MULTREAD
                     ;
                     GOCPM:
3E9E 3E04            MVI     A,04
3EAO D300            OUT     CONCTRL
3EA2 018000          LXI     B,0080H
3EAS CDOFCO          CALL    SETDMA
                     ;
                     ; SETUP LOW MEMORY ENTRIES
                     ;
3EAB 3EC3            MVI     A,JMP
3EAA 320000          STA     0
3EAD 21033E          LXI     H,WBOOTE
3EBO 220100          SHLD    1
3EB3 320500          STA     5
3EB6 210631          LXI     H,BDOS
3EB9 220600          SHLD    6
3EBC 323800          STA     7*8
3EBF 2100C0          LXI     H,0C000H
3EC2 223900          SHLD    7*8+1
3EC5 3A0400          LDA     DISKT
3EC8 4F              MOV     C,A
3EC9 C30029          JMP     CPMB
                     ;
                     MULTREAD;
3ECC CD4BCO          CALL    BUSY
3ECF 3EC3            MVI     A,0C3H
3ED1 320800          STA     RSTRTVCTR
3ED4 21EA3E          LXI     H,MULTRTN
3ED7 220900          SHLD    RSTRTVCTR+1
3EDA 2A4000          LHLD    BFRPTR
3EDD 3E9C            MVI     A,09CH          ;MULTIPLE SECTOR COMMAND
3EDF FB              EI
3EE0 D380            OUT     COMM
```

```
                MRLP:
3EE2 76                 HLT
3EE3 DB83               IN      DATA
3EE5 77                 MOV     M,A
3EE6 23                 INX     H
3EE7 C3E23E             JMP     MRLP
                MULTRTN:
3EEA 33                 INX     SP
3EEB 33                 INX     SP
3EEC DB82               IN      SECTREG
3EEE FE1B               CPI     27
3EF0 CB                 RZ
3EF1 DB81               IN      TRACK
3EF3 B7                 ORA     A
3EF4 CA033E             JZ      WBOOTE
3EF7 C38D3E             JMP     READ1
                PMSG:
3EFA 7E                 MOV     A,M
3EFB B7                 ORA     A
3EFC C8                 RZ
3EFD 4F                 MOV     C,A
3EFE CD1E3F             CALL    CONOUT
3F01 23                 INX     H
3F02 C3FA3E             JMP     PMSG
                CONST:
3F05 DB00               IN      CONCTRL
3F07 E640               ANI     40H
3F09 C8                 RZ
3F0A 3EFF               MVI     A,0FFH
3F0C C9                 RET
                CONIN:
3F0D CD053F             CALL    CONST
3F10 B7                 ORA     A
3F11 CA0D3F             JZ      CONIN
3F14 DB01               IN      1
3F16 E67F               ANI     7FH
3F18 FE5F               CPI     UNDERLINE       ;HANDY FOR ADM-3
3F1A C0                 RNZ
3F1B 3E7F               MVI     A,RUBOUT
3F1D C9                 RET
                CONOUT:
3F1E DB00               IN      CONCTRL
3F20 E680               ANI     80H
3F22 CA1E3F             JZ      CONOUT
3F25 79                 MOV     A,C
3F26 FE1A               CPI     1AH             ;MASK CLEAR SCREEN
3F28 C8                 RZ
3F29 D301               OUT     1
3F2B C9                 RET
                LIST:
3F2C DB08               IN      8
3F2E E680               ANI     80H
3F30 CA2C3F             JZ      LIST
```

```
3F33 79              MOV     A,C
3F34 D309            OUT     9
3F36 FEOC            CPI     FF
3F38 CO              RNZ
3F39 OEOO            MVI     C,O
3F3B 0642            MVI     B,66
             STALL:                              ;WAIT FOR FORM FEED
3F3D CD2C3F          CALL    LIST
3F40 05              DCR     B
3F41 C23D3F          JNZ     STALL
3F44 C9              RET

3F1E =       PUNCH   EQU     CONOUT
3FOD =       READER  EQU     CONIN
C003 =       HOME    EQU     0C003H
C006 =       SELDSK  EQU     0C006H
C009 =       SETTRK  EQU     0C009H
C00C =       SETSEC  EQU     0C00CH
C00F =       SETDMA  EQU     0C00FH
C012 =       READ    EQU     0C012H
C015 =       WRITE   EQU     0C015H
C04B =       BUSY    EQU     0C04BH              ;CHECK THIS IN YOUR DOCUMENT
000D =       CR      EQU     ODH
000A =       LF      EQU     OAH
0080 =       STATUS  EQU     0080H               ;BASE ADDRESS FOR CONTROL
                                                 ;I/O PORTS IN MY SYSTEM
0080 -       COMM    EQU     0080H
0081 =       TRACK   EQU     0081H
0082 =       SECTREG EQU     0082H
0083 =       DATA    EQU     0083H
0084 =       DEVSEL  EQU     0084H               ;THIS ONE ADDRESSED
                                                 ;SEPARATELY
0040 =       BFRPTR  EQU     0040H               ;ANY TWO EMPTY BYTES
0008 =       RSTRTN  EQU     0008H               ;I USE RESTART 1, ANY
                                                 ; WILL DO--YOU CHOOSE
0004 =       DISKT   EQU     4
0000 =       CONCTRL EQU     0
2900 =       CPMB    EQU     CPMBASE+128
0008 -       RSTRTVCTR       EQU     RSTRTN
000C =       FF      EQU     OCH
007F =       RUBOUT  EQU     7FH
005F =       UNDERLINE       EQU     5FH

             ;THESE ARE THE PROGRAMS INCLUDED IN THE 2708 ON THE FDC-1
             ; DISK CONTROLLER, AND THEIR STARTING ADDRESSES.

C000                 ORG     0C000H              ; COMPLETELY ARBITRARY

             ; JUMP TABLE FOR EASY ENTRY

C000 C321C0          JMP     BOOT                ;READS TRK 0 SCTR 1 INTO
C003 C357C0          JMP     HOME                ;RESETS CONTROLLER
C006 C322C1          JMP     SELDSK              ;KEEPS TRACK OF 2 DRIVES
```

```
C009 C36CC0          JMP     SETTRK
C00C C391C0          JMP     SETSEC
C00F C39BC0          JMP     SETDMA          ;DATA ADDRESS IN MEMORY
C012 C3A4C0          JMP     READSEC
C015 C3CBC0          JMP     WRITESEC
C018 C38EC1          JMP     FORMAT          ;SINGLE TRACK FORMAT
C01B C33AC1          JMP     GETSYS          ;FOR PATCHING CPM
C01E C340C1          JMP     PUTSYS
```

V. GENERAL

V-1. The WAMECO INCORPORATED product you have purchased is guaranteed for a period of ninety (90) days from date of purchase from your dealer against defects in manufacturing. Upon receipt of the defective board by WAMECO INCORPORATED, pre-paid freight or mailing, the board will be cheerfully replaced and the shipping charges incurred by you will be repaid. The guaranty is limited to replacement of the board with an equivalent board even though the board may be defective through negligence in manufacturing or through other fault.

V-2. For future reference, a print of the front and back traces of the FDC-1 is shown (see figures A and B).

V-3. We sincerely hope that the FDC-1 will give you long and satisfactory service. If you have any problems with the FDC-1, or if you just want to comment on the board, please write to me personally.

Chuck Naegeli

Chuck Naegeli
President
WAMECO INCORPORATED
111 Glenn Way #8
Belmont, CA 94002

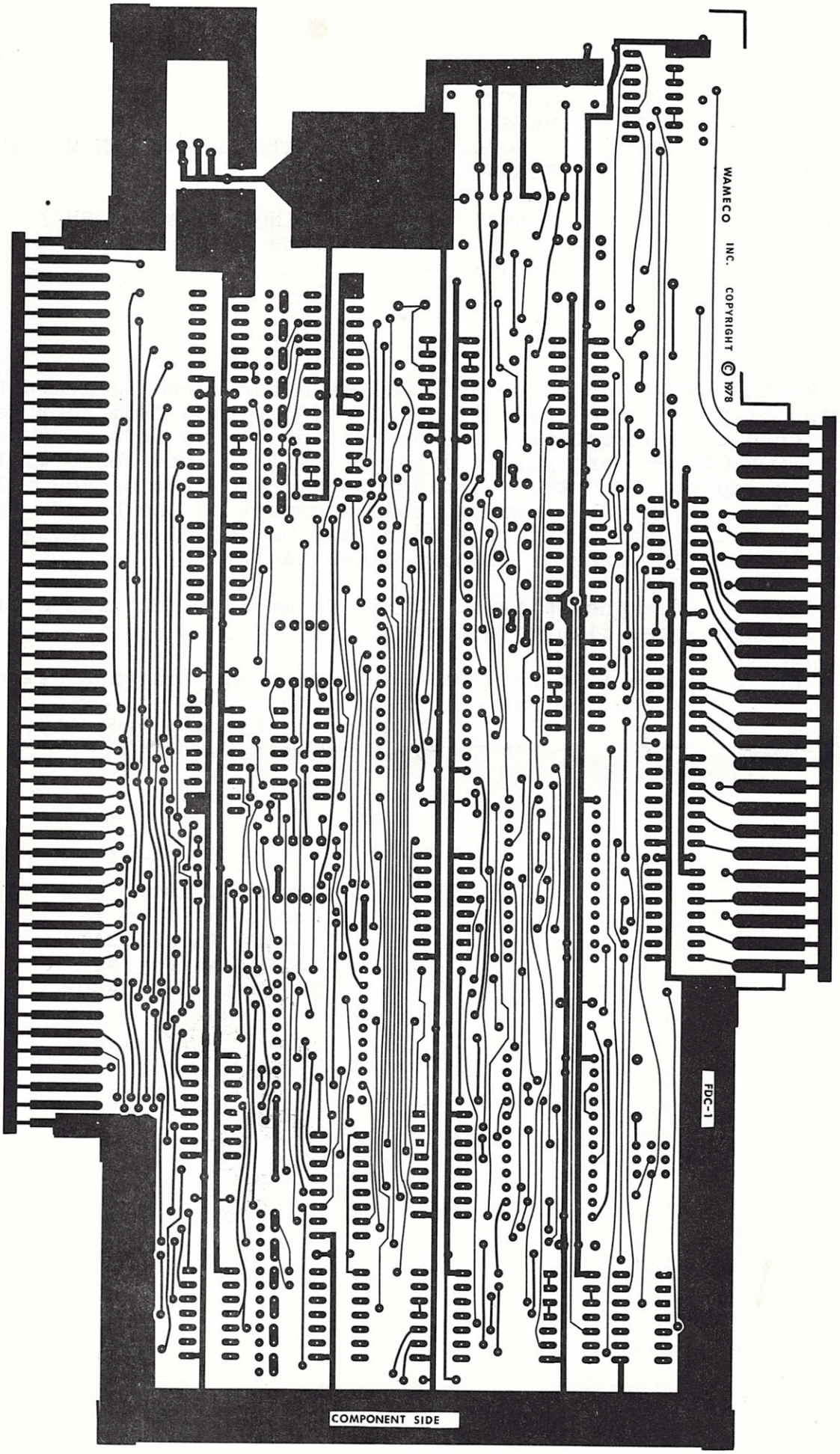


Figure A. FDC-1 component side of board

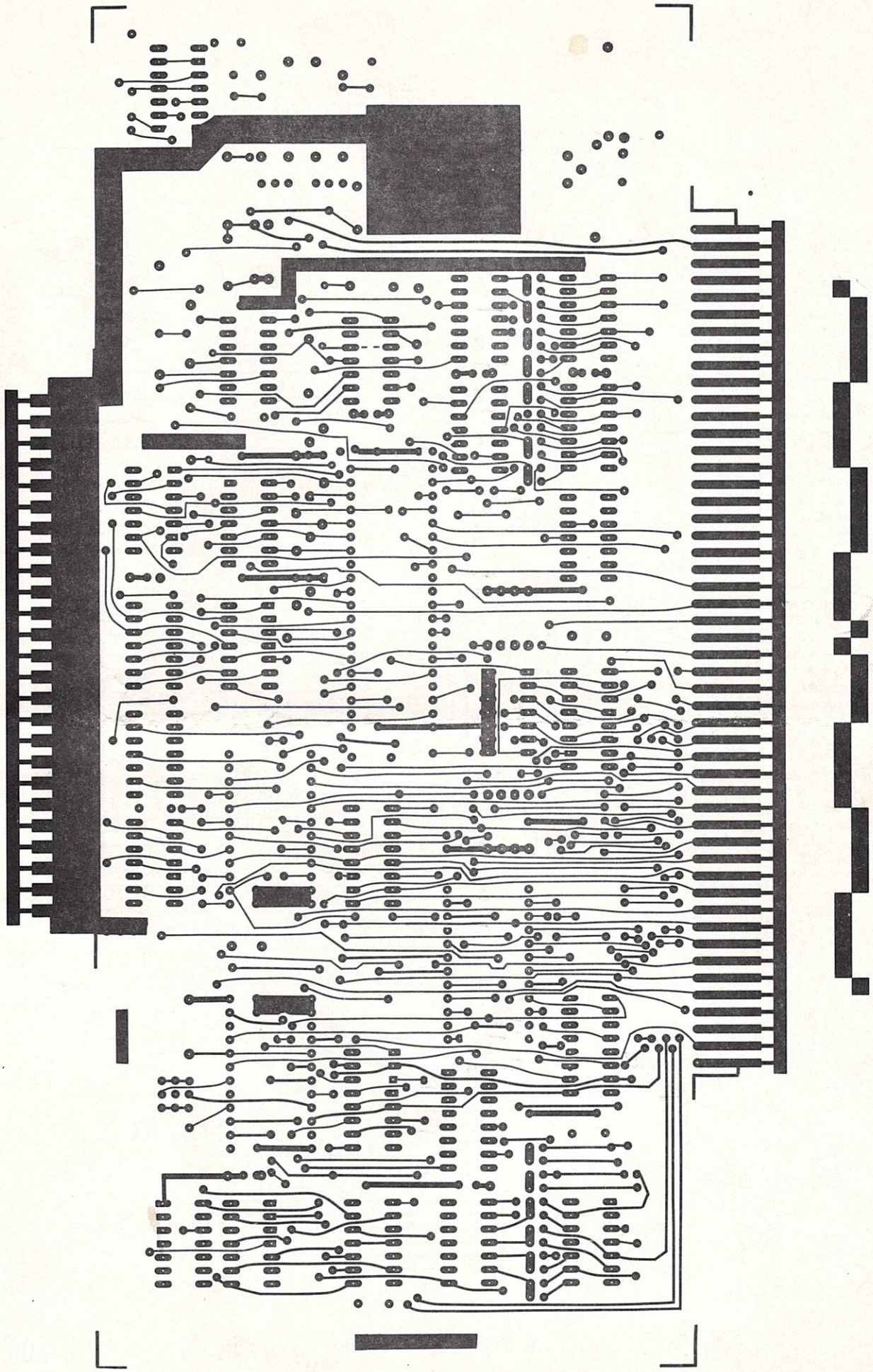


Figure B. FDC-1 trace side of board

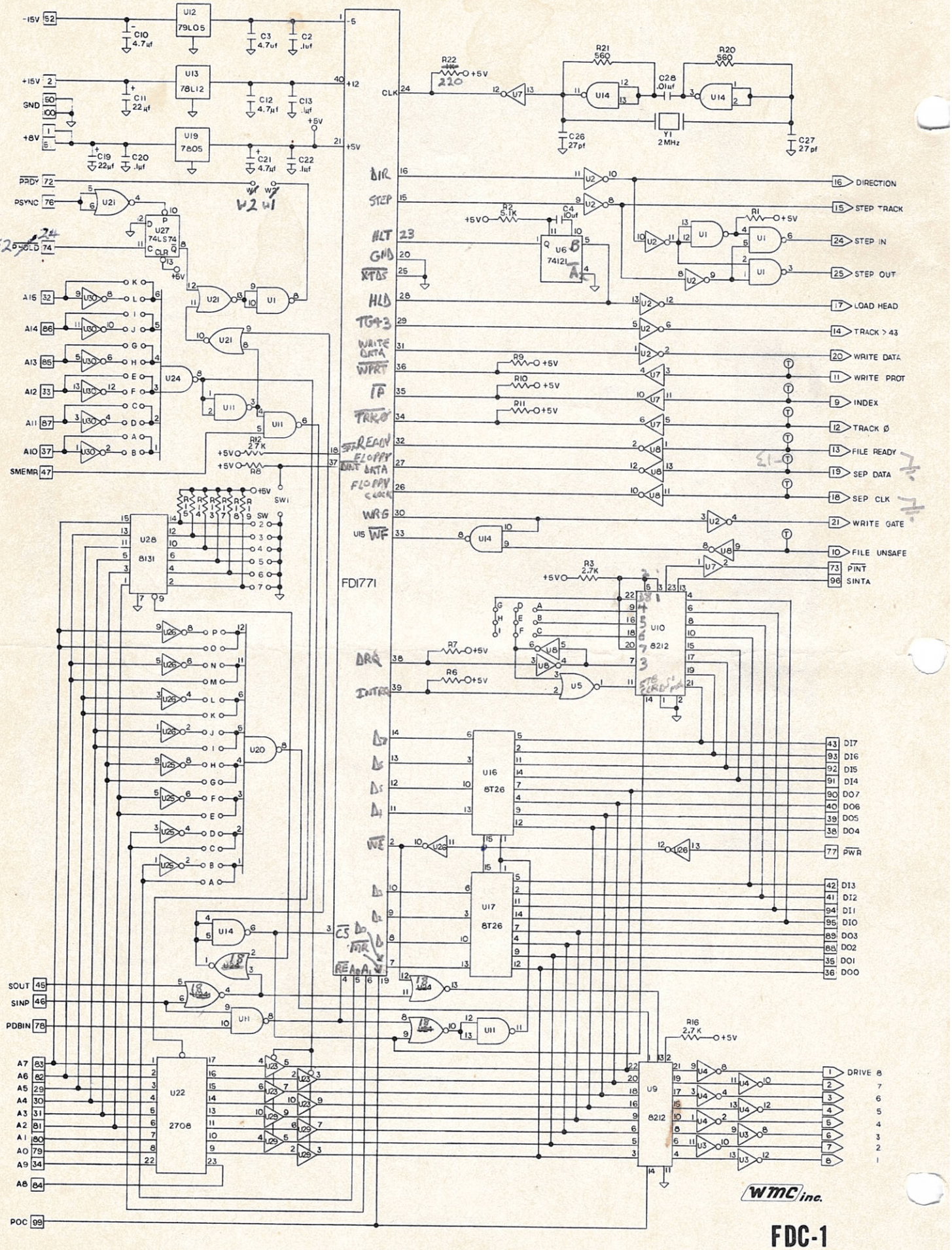
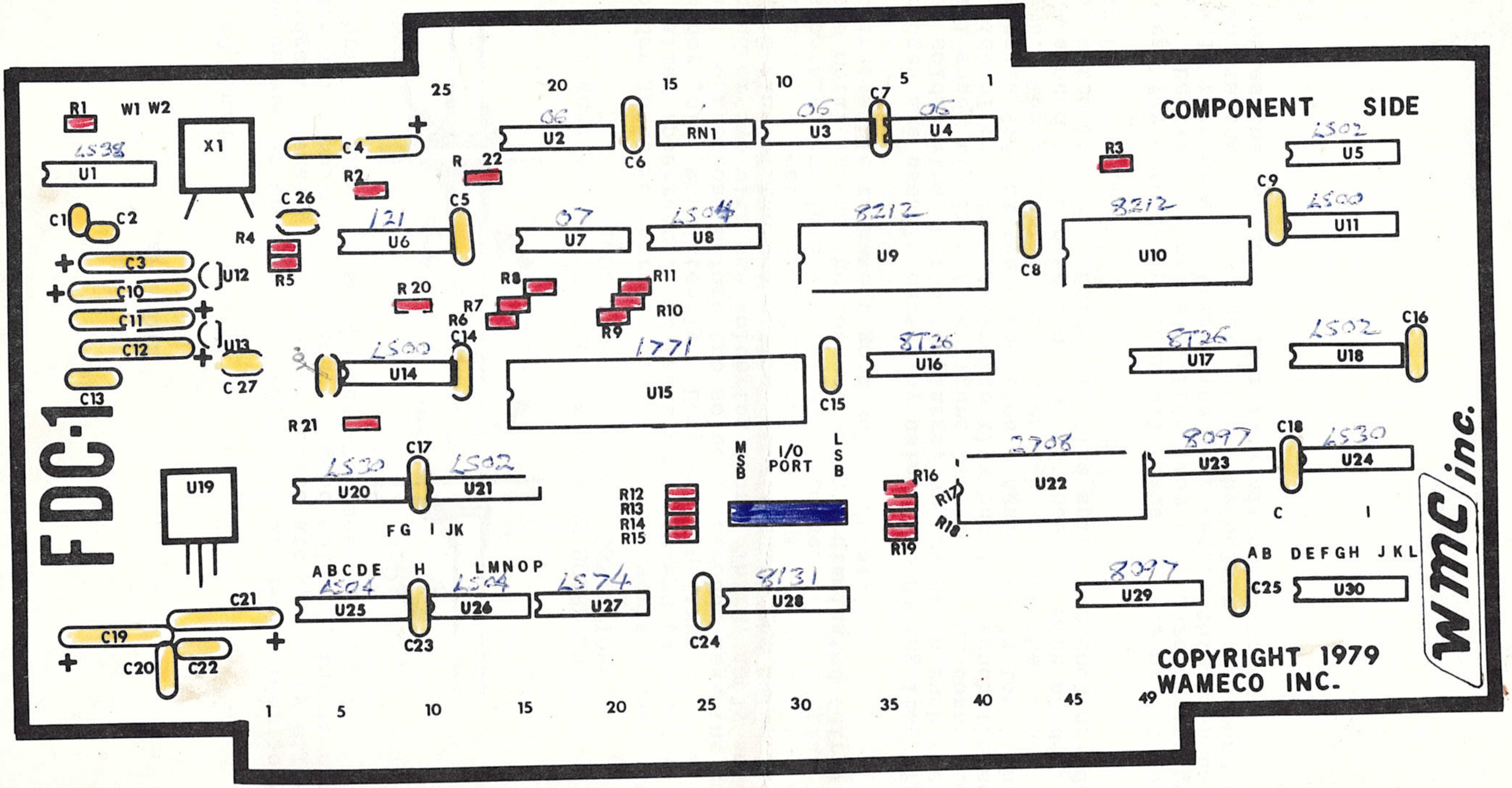


Figure 2 FDC-1 Schematic Diagram


FDC-1
COMPONENT SIDE
COPYRIGHT 1979
WAMECO INC.
WMC inc.
I/O PORT
MSB
LSB

APPENDIX A

Soldering PC Boards

Two common causes of trouble with PC boards are bad solder joints or solder bridges. Usually, bad solder joints are caused by either a cold solder joint or contamination. A good solder joint is characterized by a bright shiny and smooth surface (see figure 1).

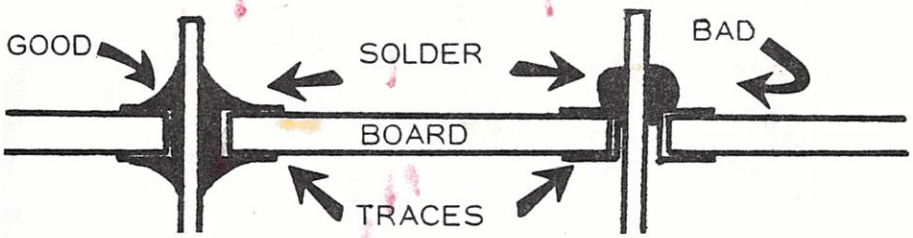


Figure A1. CROSS-SECTION OF A PC BOARD SHOWING GOOD AND BAD SOLDER CONNECTIONS

A cold solder joint is characterized by a dull surface and usually a lumpy or balled appearance. It takes practice and patience to obtain a good solder joint consistently. However, the first step is to apply flux to all connections before the solder. Second, heat the connection for a second or two with the soldering iron. Third, apply solder to the opposite side of the connection. Don't touch the solder to the iron. Flux has a "wetting" effect on solder which causes the solder to flow smoothly, completely filling the connection. If flux is not used or the metal around the connection is contaminated (dirty), it is almost impossible to have a good solder joint.

Solder bridges are usually caused by using a soldering iron tip that's too large, solder wire that's too large, or trying to rush the job. Use a small spade tip iron (see figure 2). Touch the connection with the flat side of the tip. After the flux bubbles, touch the solder to the opposite side of the connection. Again, don't touch the solder to the iron. The connection is hot enough to melt the solder causing it to flow around the connection. Do not use too much solder. Use a little and watch it flow. Solder is like spice for cooking--don't use too much.

Applying heat for extended periods will cause either or both of the following: the trace or pad will lift from the board or the board material will turn brown. Remove the iron before this happens. One hobbyist counts the bubbles that pop in the solder. He found seven to nine bubbles insured good solder flow without overheating.

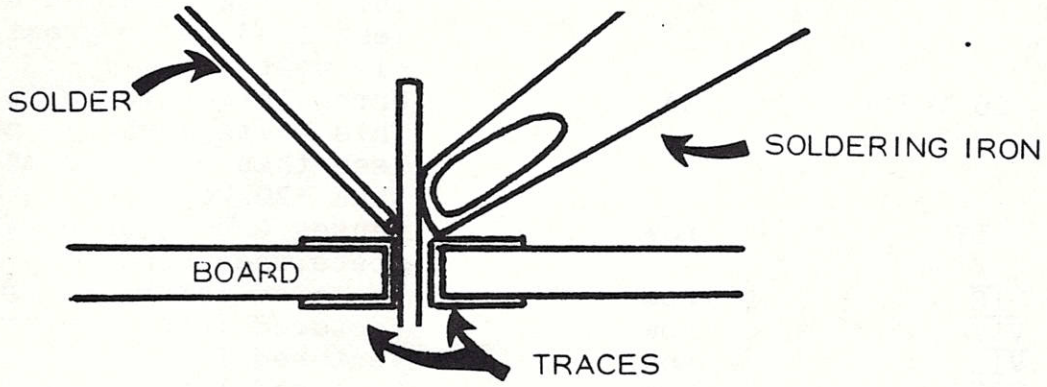


Figure 2.

Pin #	Mnemonic	Enabled State	Description
1	+8 Volts	NA	Unregulated +8 Volts DC. This voltage should not be less than +8 or greater than +11 volts.
2	+16 Volts	NA	Unregulated +16 Volts DC. This Voltage should not be less than +16 or greater than +20 Volts
3	XRDY	Low	Causes CPU to enter WAIT state when enabled.
4	$\overline{\text{V10}}$	Low	Vectored Interrupt priority 0
5	$\overline{\text{V11}}$	Low	Vectored Interrupt priority 1
6	$\overline{\text{V12}}$	Low	Vectored Interrupt priority 2
7	$\overline{\text{V13}}$	Low	Vectored Interrupt priority 3
8	$\overline{\text{V14}}$	Low	Vectored Interrupt priority 4
9	$\overline{\text{V15}}$	Low	Vectored Interrupt priority 5
10	$\overline{\text{V16}}$	Low	Vectored Interrupt priority 6
11	$\overline{\text{V17}}$	Low	Vectored Interrupt priority 7
12	---	NA	Not used
13	---	NA	Not used
14	---	NA	Not used
15	---	NA	Not used
16	---	NA	Not used
17	STAT DISABLE	Low	The eight status line buffers on the CPU board enter the high impedance state when enabled.
19	C/C DISABLE	Low	The six command/control line buffers on the CPU board enter the high impedance state when enabled.
20	UNPROTECT	High	Combined with address in an AND gate on a memory board which causes the PROTECT flip-flop to be cleared.
21	SS	High	Indicates the CPU is single stepping.
22	$\overline{\text{ADDR DSBL}}$	Low	The 16 address line buffers on the CPU board enter the high impedance state when enabled.
23	$\overline{\text{DO DSBL}}$	Low	The eight data-out lines on the CPU board enter the high impedance state when enabled.
24	Ø 2	High	Buffered TTL CPU phase 2 clock
25	Ø 1	High	Buffered TTL CPU phase 1 clock
26	PHLDA	High	CPU board "Hold Acknowledge" to HOLD-H input.
27	PWAIT	High	CPU output showing a WAIT state is occurring.

Figure A-3

Pin #	Mnemonic	Enabled State	Description
28	PINTE	High	CPU output showing that Interrupts are enabled.
29	A5 High	High	Address Bit 5
30	A4	High	Address Bit 4
31	A3	High	Address Bit 3
32	A15	High	Address Bit 15
33	A12	High	Address Bit 12
34	A9	High	Address Bit 9
35	DO1	High	CPU Data Out Bit 1
36	DO	High	CPU Data Out Bit 0
37	A10	High	Address Bit 10
38	DO4	High	CPU Data Out Bit 4
39	DO5	High	CPU Data Out Bit 5
40	DO6	High	CPU Data Out Bit 6
41	D12	High	Data In Bit 2 to CPU
42	D13	High	Data In Bit 3 to CPU
43	D17	High	Data In Bit 7 to CPU
44	SM1	High	CPU output indicating it is performing Fetch Instruction.
45	SOUT	HIgh	CPU output showing it is in an output cycle.
46	SINP	High	CPU output showing it is in an input cycle.
47	SMEMR	High	CPU status signal indicating the current cycle is a Memory Read cycle.
48	SHLTA	High	CPU status signal indicating the CPU is halted.
49	CLOCK(2MHz)	Low	A buffered 2 MHz clock for general use.
50	GND	NA	Ground (common)
51	=8 Volts	NA	(Same as pin 1)
52	=16 Volts	NA	Unregulated -16 Volts DC. This voltage should not be greater than -16 or less than -20 Volts.
53	$\overline{\text{SSW DSB}}$	Low	Sense Switch Disable disables CPU board data input buffers so that CPU can read sense switches.
54	$\overline{\text{EXT CLR}}$	Low	Front panel generated I/O clear signal.
55	---	NA	Not Used
56	---	NA	Not Used
57	---	NA	Not Used
58	---	NA	Not Used
59	---	NA	Not Used
60	---	NA	Not Used
61	---	NA	Not Used

S-100 (WAMECO) BUS DESCRIPTION (Cont.)

Pin #	Mnemonic	Enabled State	Description
62	---	NA	Not Used
63	---	NA	Not Used
64	---	NA	Not Used
65	---	NA	Not Used
66	---	NA	Not Used
67	PHANTOM	NA	Used for Memory Bank Selection (or for SOL Systems)
68	MWRITE	High	CPU output showing Data Out Bus data is to be written into the memory selected by the address lines
69	$\overline{PS}$	Low	Shows Protect Status of selected memory.
70	PROTECT	High	Combined with address in an AND gate on a memory board which causes the PROTECT flip-flop to be set.
71	RUN	High	Front panel indication that CPU run instruction has been input.
72	PRDY	Low	Causes the CPU to enter the WAIT state when enabled.
73	$\overline{PINT}$	Low	If interrupts have been enabled causes the CPU to enter the Interrupt Acknowledge condition at the conclusion of the current instruction.
74	$\overline{PHOLD}$	Low	CPU input which causes a HOLD status to occur. DMA transfer request signal is PHOLD.
75	$\overline{PRESET}$	Low	CPU board system reset signal.
76	PSYNC	High	CPU output showing the start of a new machine cycle. This signal is used on the CPU board to enable the loading of the System Status Latch.
77	$\overline{PWR}$	Low	Indication that data on the Data Out Bus is to be written either to a memory or an I/O device.
78	PDBIN	Low	Indication to the selected memory or I/O device that the CPU expects data on the Data In Bus.
79	AO	High	Address Bit 0
80	A1	High	Address Bit 1
81	A2	High	Address Bit 2
82	A6	High	Address Bit 6

S-100 (WAMECO) BUS DESCRIPTION (Cont.)

Pin #	Mnemonic	Enabled State	Description
83	A7	High	Address Bit 7
84	A8	High	Address Bit 8
85	A13	High	Address Bit 13
86	A14	High	Address Bit 14
87	A11	High	Address Bit 11
88	DO2	High	CPU Data Out Bit 2
89	DO3	High	CPU Data Out Bit 3
90	DO7	High	CPU Data Out Bit 7
91	D14	High	Data In Bit 4 to CPU
92	D15	High	Data In Bit 5 to CPU
93	D16	High	Data In Bit 6 to CPU
94	D11	High	Data In Bit 1 to CPU
95	D10	High	Data In Bit 0 to CPU
96	SINTA	High	CPU Interrupt Acknowledge Signal
97	SWO	Low	CPU output indicating the current cycle involves writing to a memory or I/O device.
98	SSTACK	High	CPU output indicating the address bus contains the stack address and the current cycle will have a stack operation.
99	$\overline{\text{POC}}$	Low	Power On Clear reset signal
100	GND	NA	Ground (common)

S-1ØØ (WAMECO) BUS DESCRIPTION

PIN	MNEMONIC	TERM.
1	+5V	
2	+15V	
3	XRDY	X
4	V10	X
5	V11	X
6	V12	X
7	V13	X
8	V14	X
9	V15	X
10	V16	X
11	V17	X
12		
13		
14		
15		
16		
17		
18	STAT DISABLE	X
19	CIC DISABLE	X
20	UNPROTECT	X
21	SS	X
22	ADDR DSBL	X
23	DO DSBL	X
24	Ø 2	X
25	Ø 1	X
26	PHLDA	X
27	PWAIT	
28	PINTE	
29	A5	
30	A4	
31	A3	
32	A15	
33	A12	
34	A9	
35	DO1	X
36	DOØ	X
37	A10	
38	DO4	X
39	DO5	X
40	DO6	X
41	D12	X
42	D13	X
43	D17	X
44	SMI	
45	SOUT	
46	SINP	
47	SMEMR	
48	SHLTA	
49	CLOCK (2 MHz)	
50	GND	

PIN	MNEMONIC	ALTER. PIN DESIG.	TERM.
51	+5V	A	
52	-15V	B	
53	SSW DSB	C	
54	EXT CLR	D	X
55		E	
56		F	
57		H	
58		J	
59		K	
60		L	
61		M	
62		N	
63		P	
64		R	
65		S	
66		T	
67	PHANTOM	U	
68	MWRITE	V	X
69	PS	W	
70	PROTECT	X	X
71	RUN	Y	X
72	PRDY	Z	X
73	PINT	a	X
74	PHOLD	b	X
75	PRESET	c	X
76	PSYNC	d	X
77	PWR	e	X
78	PDBIN	f	X
79	AØ	h	
80	A1	j	
81	A2	k	
82	A6	l	
83	A7	m	
84	A8	n	
85	A13	p	
86	A14	r	
87	A11	s	
88	DO2	t	X
89	DO3	u	X
90	DO7	v	X
91	D14	w	X
92	D15	x	X
93	D16	y	X
94	D11	z	X
95	DIØ	AA	X
96	SINTA	AB	
97	SWO	AC	
98	SSTACK	AD	
99	POC	AE	
100	GND	AF	

APPENDIX B

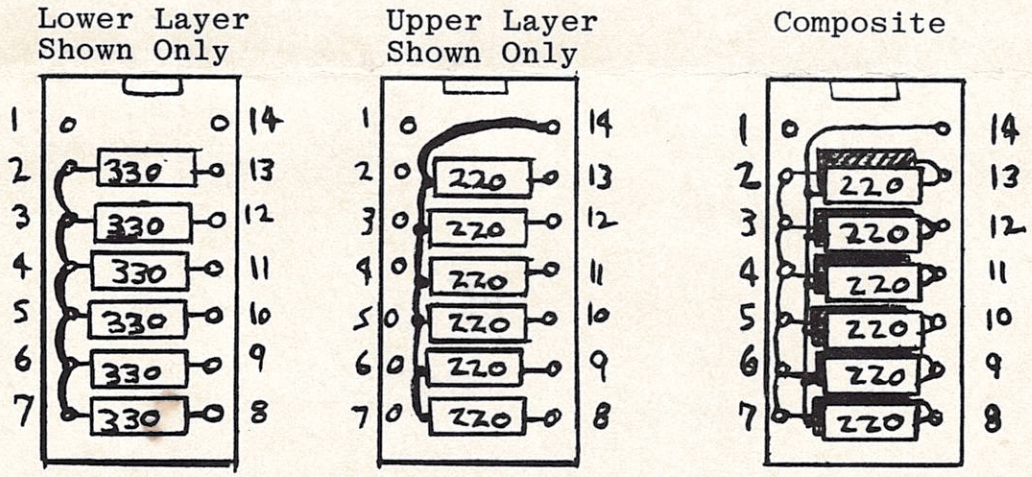
Due to the possibility of not being able to get the termination resistor pack, it may be simulated by the following assembly:

Grant Connell
2/27/79

FDC-1

Termination Header

Part # Allen-Bradley 314E221331
¼ watt resistors



The above drawings show a single header with two layers.

APPENDIX C

```
                ;
                ; THIS IS THE PROGRAM TO BE PLACED IN THE 2708 FOR
                ; THE WAMECO INC. FDC-1 DISK CONTROLLER.
                ;
                ;  COPYRIGHT 1979, WAMECO INC.
                ;
C000                    ORG     0C000H          ; COMPLETELY ARBITRARY

                ; JUMP TABLE FOR EASY ENTRY

C000 C327C0             JMP     BOOT            ;READS TRK 0 SCTR 1 INTO 0000H
C003 C35DC0             JMP     HOME            ;RESETS CONTROLLER
C006 C357C1             JMP     SELDSK          ;KEEPS TRACK OF 2 DRIVES
C009 C372C0             JMP     SETTRK
C00C C397C0             JMP     SETSEC
C00F C3A1C0             JMP     SETDMA          ;DATA ADDRESS IN MEMORY
C012 C3AAC0             JMP     READSEC
C015 C300C1             JMP     WRITESEC
C018 C3C3C1             JMP     FORMAT          ;SINGLE TRACK FORMAT
C01B C36FC1             JMP     GETSYS          ;FOR PATCHING CPM
C01E C375C1             JMP     PUTSYS
C021 C351C0             JMP     BUSY
C024 C3CFC0             JMP     READTRK         ;FOR BOOT--A FULL TRACK IN 1 REV

                BOOT:
C027 310001             LXI     SP,100H
C02A AF                 XRA     A
C02B 320400             STA     DISKT           ;SET DRIVE A
C02E 3EC3               MVI     A,0C3H          ;SET ERROR RETURN
C030 320800             STA     RSTRTN
C033 2127C0             LXI     H,BOOT
C036 220900             SHLD    9
C039 CD5DC0             CALL    HOME            ,TRACK 0
C03C 0E01               MVI     C,1             ;SECTOR 1
C03E CD97C0             CALL    SETSEC
C041 210000             LXI     H,0             ;DATA TO 0000H
C044 3E8C               MVI     A,RDCOMM
C046 FB                 EI
C047 D380               OUT     COMM
                BOOTLUP:
C049 76                 HLT
C04A DB83               IN      DATA
C04C 77                 MOV     M,A
C04D 23                 INX     H
C04E C349C0             JMP     BOOTLUP

                ; THIS ROUTINE ENDS WITH AN OPERATION COMPLETE INTERRUPT
                ; WHICH TRANSFERS CONTROL TO RAM ADDRESS 0008H



                ; THIS FIRST ROUTINE IS USED BY ALL THE OTHERS TO LET THE
                ; CONTROLLER FINISH ITS CURRENT TASK BEFORE BEGINNING ANOTHER.

                BUSY:
```

```
C051 F3              DI
C052 CD4AC1          CALL    SELECT
C055 DB80            IN      STATUS          ;SEE IF DRIVE IS READY
C057 E681            ANI     0081H           ;AND BUSY
C059 C8              RZ                      ;READY AND WAITING
C05A C355C0          JMP     BUSY+4          ;JUST WAIT HERE

                ; THIS ROUTINE RESETS THE CONTROLLER BOARD AND MOVES THE
                ; HEAD TO TRACK 0.

C05D CD51C0     HOME    CALL    BUSY            ;SEE IF BUSY
C060 3E02               MVI     A,2             ;RESTORE WITH 10MS/STEP
C062 D380               OUT     COMM            ;0 IS A HOME COMMAND
C064 CD55C0             CALL    BUSY+4          ;WAIT TIL FINNISHED
C067 DB80               IN      STATUS          ,CHECK TO SEE IF WE
C069 E604               ANI     TRK0            ,MADE IT TO ZERO
C06B CA5DC0             JZ      HOME
C06E CD51C1             CALL    DESELECT
C071 C9                 RET

                ; THIS ROUTINE SEEKS TO THE TRACK IN THE C-REGISTER.
                ; UPON RETURN, ACCUMULATOR CONTAINS ANY EOC3H   FLAGS.

                SETTRK:
C072 DB81               IN      TRACK
C074 B9                 CMP     C
C075 C27AC0             JNZ     TRK2
C078 AF                 XRA     A
C079 C9                 RET
                TRK2:
C07A CD82C0             CALL    SEEK
C07D B7                 ORA     A
C07E C8                 RZ
C07F CD5DC0             CALL    HOME
C082 CD51C0     SEEK    CALL    BUSY            ;CAN'T DO 2 THINGS AT ONCE
C085 79                 MOV     A,C             ;GET TRACK NUMBER
C086 D383               OUT     DATA            ;GIVE TO CONTROLLER
C088 CD55C0             CALL    BUSY+4          ,LET IT MUNCH
C08B 3E16               MVI     A,SKCOMM        ;GENERATE SEEK COMMAND
C08D D380               OUT     COMM            ,WITH VERIFY FLAG, ETC..
C08F CD55C0             CALL    BUSY+4          ;THIS COULD TAKE A WHILE
C092 DB80               IN      STATUS          ;CHECK FOR ERRORS
C094 E610               ANI     SKERR           ,STRIP THE GARBAGE
C096 C9                 RET                     ;BYE!

                ; THIS ROUTINE SELECTS THE SECTOR FOR SUBSEQUENT OPERATIONS
                ; THAT IS DESCRIBED BY THE C-REGISTER.

C097 CD51C0     SETSEC  CALL    BUSY            ;SAME OLD STUFF
C09A 79                 MOV     A,C
C09B D382               OUT     SECTREG         ;TELL THE CONTROLLER
C09D 2F                 CMA
C09E D3FF               OUT     OFFH            ;BLINK THE LIGHTS
C0A0 C9                 RET
                ;
                ; THIS ROUTINE ESTABLISHES THE DESTINATION ADDRESS OF
                ; THE READ DATA, OR THE SOURCE ADDRESS OF THE WRITE
                ; DATA FOR READ OR WRITE COMMANDS WHICH FOLLOW.
```

```
COA1 E5        SETDMA  PUSH    H               ;DON'T WRECK ANYTHING
COA2 214000            LXI     H,BFRPTR        ;WE STORE THE ADDRESS
COA5 71                MOV     M,C             ;FOR FUTURE REFERENCE
COA6 23                INX     H
COA7 70                MOV     M,B             ;NOTICE THE TARGET ADDRESS
COA8 E1                POP     H               ;CAME FROM THE B-C PAIR
COA9 C9                RET

                ; THIS IS THE READ ROUTINE.  THE HARDWARE FORCES AN
                ; ENABLE INTERRUPT (EI) COMMAND TO BE EXECUTED UPON
                ; RECEIPT OF A DATA REQUEST INTERRUPT INSTEAD OF THE
                ; NORMAL RESTART INSTRUCTION USUALLY ASSOCIATED WITH
                ; INTERRUPT PROCESSING.  SO WE DON'T BRANCH ANYWHERE
                ; UNTIL WE'RE DONE, WHEN THE HARDWARE DOES A RESTART.

                READSEC:
COAA CD51C0            CALL    BUSY
COAD C5                PUSH    B               ;SAVE EVERYTHING!
COAE E5                PUSH    H
COAF 3EC3              MVI     A,00C3H         ;SET UP THE VECTOR
COB1 320800            STA     RSTRTN          ;FOR WHEN WE'RE DONE
COB4 2125C1            LXI     H,RVCTR         ;IN CASE IT'S BEEN USED
COB7 220900            SHLD    RSTRTN+1
COBA 060A              MVI     B,10            ;TRY 10 TIMES FOR SOFT
COBC CD55C0    LUP1    CALL    BUSY+4          ;ERROR RECOVERY
COBF 2A4000            LHLD    BFRPTR          ;GET THE ADDRESS
COC2 3E8C              MVI     A,RDCOMM        ;SET UP BY SETDMA
COC4 FB        POINT1  EI                      ;GOT TO HAVE INTERRUPTS!
                                               ;ENTRY POINT FROM MULT READ
COC5 D380              OUT     COMM            ;MAKE IT GO!

                ; WE WAIT HERE FOR FIRST AND ALL DATA REQUESTS

COC7 76        LUP2    HLT

                ; DATA REQUEST NOW FORCES AN EI INSTRUCTION

COC8 DB83              IN      DATA            ;GRAB THAT BYTE
COCA 77                MOV     M,A             ;SALT IT AWAY
COCB 23                INX     H               ;UPDATE THE POINTER
COCC C3C7C0            JMP     LUP2            ;WAIT FOR THE NEXT ONE

                ; THE ONLY WAY WE GET OUT OF THIS ONE IS WHEN THE
                ; CONTROLLER DIFFERENTIATES BETWEEN A DATA REQUEST
                ; AND A JOB COMPLETE INTERRUPT.  THEN WE DO A RESTART TO
                ; THE RVCTR ROUTINE, WHICH FINISHES THINGS UP.

                READTRK:
COCF C5                PUSH    B
COD0 E5                PUSH    H
COD1 CD72C0            CALL    SETTRK          ;ENTER WITH TRACK NUM IN C
                AGAIN2:
COD4 0E01              MVI     C,1
COD6 CD97C0            CALL    SETSEC          ;READ FROM SECTOR 1
COD9 EB                XCHG                    ;ADDRESS IS IN D-E PAIR
CODA 224000            SHLD    BFRPTR
CODD EB                XCHG                    ;RESTORE THE WORLD
CODE 3EC3              MVI     A,JMP
COE0 320800            STA     RSTRTN
```

```
C0E3 21F1C0          LXI     H,RDTRKVTR
C0E6 220900          SHLD    RSTRTN+1
C0E9 2A4000          LHLD    BFRPTR
C0EC 3E9C            MVI     A,MRDCOMM       ;GO AND DO IT!
C0EE C3C4C0          JMP     POINT1          ;SAME LOOP AS SECTOR READ

                     RDTRKVTR:
C0F1 33              INX     SP
C0F2 33              INX     SP              ;SAME OLD STACK CORRECTION
C0F3 DB82            IN      SECTREG
C0F5 FE1B            CPI     27              ;DID WE MAKE IT TO THE END?
C0F7 C2FDC0          JNZ     AGAIN1
C0FA E1              POP     H
C0FB C1              POP     B
C0FC C9              RET
C0FD C3D4C0    AGAIN1: JMP   AGAIN2


                     ; THIS IS THE WRITE SECTOR ROUTINE. IT OPERATES
                     ; JUST LIKE THE READ ROUTINE EXCEPT WE WRITE DATA
                     ; FROM MEMORY INSTEAD OF READING INTO IT.  WE USE
                     ; THE SAME POINTER ESTABLISHED BY THE SETDMA ROUTINE.
                     ;


                     WRITESEC:
C100 CD51C0          CALL    BUSY
C103 C5              PUSH    B
C104 E5              PUSH    H
C105 3EC3            MVI     A,00C3H
C107 320800          STA     RSTRTN
C10A 2135C1          LXI     H,WVCTR         ;SET THE RETURN VECTOR
C10D 220900          SHLD    RSTRTN+1        ;FOR THE WRITE ROUTINE
C110 060A            MVI     B,10
C112 CD55C0    LUP3  CALL    BUSY+4
C115 2A4000          LHLD    BFRPTR          ;POINTS TO WRITE DATA
C118 3EAC            MVI     A,WRTCOM
C11A FB              EI                      ;DON'T FORGET THIS!
C11B D380            OUT     COMM            ;DO IT!!
C11D 76        LUP4  HLT

                     ; AS BEFORE, WE WAIT FOR DATA REQUEST, WHICH FORCES
                     ; AN EI INSTRUCTION TO BE EXECUTED.  (THE 8080 DISABLES
                     ; INTERRUPTS IN RESPONSE TO AN INTERRUPT.)

C11E 7E              MOV     A,M             ;GET THE BYTE, NOT PUT IT
C11F D383            OUT     DATA            ,NOW PUT IT!
C121 23              INX     H               ;UPDATE POINTER
C122 C31DC1          JMP     LUP4            ;WAIT FOR NEXT ONE

                     ; WHEN WE ARE DONE, OR IN EVENT OF ERROR, RESTART WILL
                     ; END THIS ROUTINE AND PUT US IN WVCTR.


                     ; THIS IS THE DESTINATION OF THE READ RESTART INTERRUPT
                     ; WHICH OCCURS AT THE END OF THE READ OPERATION.

C125 33        RVCTR INX     SP
C126 33              INX     SP              ;ONE CALL TOO MANY
C127 DB80            IN      STATUS
```

FULL SIZE! should be 13 H (19 10)

```
C129 E69C               ANI     009CH           ;CHECK THE ERROR FLAGS
C12B CA44C1             JZ      WRTN            ;OUT IF NO MISTAKES
C12E 05                 DCR     B               ;TRY AGAIN?
C12F C2BCC0             JNZ     LUP1
C132 C342C1             JMP     WRTN-2

                ; THIS IS THE DESTINATION OF THE WRITE RESTART
                ; INTERRUPT WHICH OCCURS AT THE END OF THE WRITE
                ; OPERATION.  VERY LITTLE DIFFERENCE FROM THE READ.

C135 33         WVCTR   INX     SP              ;CORRECT THE STACK
C136 33                 INX     SP
C137 DB80               IN      STATUS          ;HOW'D WE DO?
C139 E6FC               ANI     00FCH
C13B CA44C1             JZ      WRTN            ;DID OK, GET OUT
C13E 05                 DCR     B               ;10 TRIES UP?
C13F C212C1             JNZ     LUP3
C142 3E01               MVI     A,1             ;SET ERROR FLAG
C144 E1         WRTN    POP     H
C145 C1                 POP     B               ;GET THE REGS BACK
C146 CD51C1             CALL    DESELECT
C149 C9                 RET
                ;


                ; THIS ROUTINE IS A DRIVE SELECT ROUTINE.

                SELECT:
C14A 3A0400             LDA     DISKT           ;WHERE CPM KEEPS DRIVE NO.
C14D 3C                 INR     A               ;WAS A 1 OR A 0
C14E D384               OUT     DEVSEL          ;NOW A 1 OR A 2 BIT
C150 C9                 RET
                DESELECT:
C151 F5                 PUSH    PSW
C152 AF                 XRA     A               ;TURNS ALL DRIVES OFF
C153 D384               OUT     DEVSEL
C155 F1                 POP     PSW
C156 C9                 RET
                SELDSK:
C157 3A0400             LDA     DISKT
C15A B9                 CMP     C
C15B C8                 RZ
C15C 79                 MOV     A,C
C15D 320400             STA     DISKT
C160 E5         UPDATE  PUSH    H               ;WE STORE IN RAM LOCN 42H
C161 C5                 PUSH    B               ;THE TRACK ADDRESS OF THE
C162 214200             LXI     H,0042H         ;DESELECTED DRIVE.  WE
C165 DB81               IN      TRACK           ;UPDATE THE TRACK REGISTER
C167 46                 MOV     B,M             ;WITH THE TRACK LOCN OF
C168 77                 MOV     M,A             ;THE NEWLY SELECTED DRIVE.
C169 78                 MOV     A,B             ;POWER UP UNCERTAINTY IS SOLVED
C16A D381               OUT     TRACK           ,BY SETTRK ROUTINE
C16C C1                 POP     B
C16D E1                 POP     H
C16E C9                 RET

                GETSYS:
C16F 21AAC0             LXI     H,READSEC
C172 C378C1             JMP     DOIT
```

```
                PUTSYS:
C175 2100C1             LXI     H,WRITESEC
                DOIT:
C178 310002             LXI     SP,200H
C17B 220001             SHLD    100H            ;ARBITRARY BUFFER
                DOSYS:
C17E AF                 XRA     A               ;DO IT ON DRIVE A
C17F 320400             STA     DISKT
C182 318000             LXI     SP,80H
C185 CD5DC0             CALL    HOME            ;GET TRACK 0 FIRST
C188 218028             LXI     H,CPMBASE       ;TARGET RAM ADDRESS
C18B CD9FC1             CALL    DOTRACK
                RUTIN1:
C18E 0E01               MVI     C,1             ;NOW GET TRACK 1
C190 CD72C0             CALL    SETTRK
C193 218035             LXI     H,CPMBASE+26*128  <- should be 18*128
C196 CD9FC1             CALL    DOTRACK
C199 CD51C1             CALL    DESELECT        ;DONE WITH DISK DRIVE
C19C C39CC1     FRVR:   JMP     FRVR            ;NONDESCRIPT ENDING

                DOTRACK:
C19F 224000             SHLD    BFRPTR          ;USE THIS LATER
C1A2 0E01               MVI     C,1             ;START WITH SECTOR 1
                LOOOP:
C1A4 CD97C0             CALL    SETSEC
C1A7 21AFC1             LXI     H,DUNHERE       ;SNEAKY CALL ROUTINE
C1AA E5                 PUSH    H
C1AB 2A0001             LHLD    100H            ;DETERMINED BY ENTRY
C1AE E9                 PCHL
                DUNHERE:
C1AF 118000             LXI     D,128
C1B2 2A4000             LHLD    BFRPTR
C1B5 19                 DAD     D
C1B6 224000             SHLD    BFRPTR          ;UPDATE FOR SECTOR SIZE
C1B9 DB82               IN      SECTREG         ;CHECK FOR DONE
C1BB 3C                 INR     A
C1BC FE1B               CPI     27  <-          FULL=27,0 (1BH)  MINI=18,0 (13H)
C1BE 4F                 MOV     C,A
C1BF C2A4C1             JNZ     LOOOP
C1C2 C9                 RET


                ;THIS IS A SUBROUTINE WHICH WILL FORMAT A SINGLE TRACK.
                ;UPON RETURN, THE ACCUMULATOR WILL BE ZERO FOR NO ERRORS.

                FORMAT:
C1C3 CD51C0             CALL    BUSY
C1C6 DB81               IN      TRACK
C1C8 4F                 MOV     C,A
C1C9 1601               MVI     D,1             ;START WITH SECTOR 1
->C1CB 062E             MVI     B,46            ;B IS BYTE COUNTER
C1CD 3EC3               MVI     A,JMP           ;SET UP RETURN
C1CF 320800             STA     RSTRTN
->C1D2 2150C2           LXI     H,FMTVCTR
C1D5 220900             SHLD    RSTRTN+1
C1D8 3EF4               MVI     A,WRTRKOMM      ;WRITE TRACK COMMAND
C1DA FB                 EI
C1DB D380               OUT     COMM
                LOP1:
C1DD 76                 HLT                     28503
```

```
C1DE AF             XRA     A
C1DF D383           OUT     DATA
C1E1 05             DCR     B
C1E2 C2DDC1         JNZ     LOP1
C1E5 3EFC           MVI     A,0FCH          ;INDEX MARK CODE
C1E7 76             HLT
C1E8 D383           OUT     DATA
C1EA AF             XRA     A
C1EB 061A           MVI     B,26
                LOP2:
C1ED 76             HLT
C1EE D383           OUT     DATA
C1F0 05             DCR     B
C1F1 C2EDC1         JNZ     LOP2
                SECLOOP:
C1F4 0606           MVI     B,6
                LOP3:
C1F6 76             HLT
C1F7 AF             XRA     A
C1F8 D383           OUT     DATA
C1FA 05             DCR     B
C1FB C2F6C1         JNZ     LOP3
C1FE 76             HLT
C1FF 3EFE           MVI     A,0FEH          ;ADDRESS MARK
C201 D383           OUT     DATA
C203 76             HLT
C204 79             MOV     A,C             ;GET TRACK NUMBER
C205 D383           OUT     DATA
C207 AF             XRA     A
C208 76             HLT
C209 D383           OUT     DATA
C20B 7A             MOV     A,D             ;GET SECTOR NUMBER
C20C 76             HLT
C20D D383           OUT     DATA
C20F AF             XRA     A
C210 76             HLT
C211 D383           OUT     DATA
C213 3EF7           MVI     A,0F7H          ;CRC GENERATOR
C215 76             HLT
C216 D383           OUT     DATA
C218 0611           MVI     B,17
C21A AF             XRA     A
                LOP4:
C21B 76             HLT
C21C D383           OUT     DATA
C21E 05             DCR     B
C21F C21BC2         JNZ     LOP4
C222 3EFB           MVI     A,0FBH          ;DATA MARK
C224 76             HLT
C225 D383           OUT     DATA
C227 3EE5           MVI     A,0E5H
C229 0680           MVI     B,128
                LOP5:
C22B 76             HLT
C22C D383           OUT     DATA
C22E 05             DCR     B
C22F C22BC2         JNZ     LOP5
C232 3EF7           MVI     A,0F7H          ;CRC AGAIN
C234 76             HLT
C235 D383           OUT     DATA
```

```
C237 061A               MVI     B,26
C239 AF                 XRA     A
                LOP6:
C23A 76                 HLT
C23B D383               OUT     DATA
C23D 05                 DCR     B
C23E C23AC2             JNZ     LOP6
C241 76                 HLT
C242 D383               OUT     DATA
C244 14                 INR     D
C245 3E1B               MVI     A,27
C247 BA                 CMP     D
C248 C2F4C1             JNZ     SECLOOP
C24B AF                 XRA     A
C24C D383               OUT     DATA
C24E F3                 DI
C24F C9                 RET
                FMTVCTR:
C250 33                 INX     SP
C251 33                 INX     SP
C252 DB80               IN      STATUS
C254 E6E5               ANI     0E5H            ;ERROR FLAGS
C256 C9                 RET

                ; THIS IS THE TABLE OF CONSTANTS FOR THE ENTIRE PROGRAM

0080 =          STATUS  EQU     0080H           ;BASE ADDRESS FOR CONTROLLER
                                                ,I/O PORTS IN MY SYSTEM
0080 =          COMM    EQU     0080H
0081 =          TRACK   EQU     0081H
0082 =          SECTREG EQU     0082H
0083 =          DATA    EQU     0083H
0084 =          DEVSEL  EQU     0084H           ;THIS ONE ADDRESSED
                                                ;SEPERATELY
0004 =          TRKO    EQU     0004H
0016 =          SKCOMM  EQU     0016H           ;SEEK, VERIFY, 10MS/STEP
0010 =          SKERR   EQU     0010H           ;SEEK ERROR FLAG
0040 =          BFRPTR  EQU     0040H           ;ANY TWO EMPTY BYTES
0008 =          RSTRTN  EQU     0008H           ;I USE RESTART 1, ANY
                                                ; WILL DO--YOU CHOOSE
008C =          RDCOMM  EQU     008CH           ;IBM FORMAT, LD HEAD, 1 SECTOR
00AC =          WRTCOM  EQU     00ACH           ,SAME AS READ SPECS
0004 =          DISKT   EQU     4               ;CPM'S ASSIGNMENT
0008 =          RSTRTVCTR       EQU     RSTRTN
009C =          MRDCOMM EQU     9CH
00BC =          MWRTCOMM        EQU     0BCH
2880 =          CPMBASE EQU     2880H           ;16K BASE ADDRESS FOR CPM
00F4 =          WRTRKOMM        EQU     0F4H    ,USED ONLY FOR FORMATTING

A>
```