

## Soldering PC Boards

Two common causes of trouble with PC boards are bad solder joints or solder bridges. Usually, bad solder joints are caused by either a cold solder joint or contamination. A good solder joint is characterized by a bright shiny and smooth surface ( see figure 1).

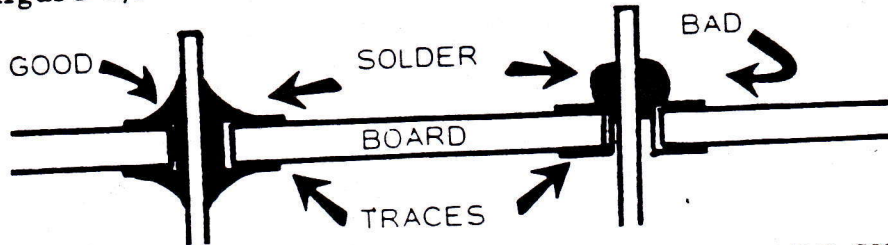


Figure 1. CROSS-SECTION OF A PC BOARD SHOWING GOOD AND BAD SOLDER CONNECTIONS

A cold solder joint is characterized by a dull surface and usually a lumpy or balled appearance. It takes practice and patience to obtain a good solder joint consistently. However, the first step is to apply flux to all connections before the solder. Second, heat the connection for a second or two with the soldering iron. Third, apply solder to the opposite side of the connection. Don't touch the solder to the iron. Flux has a "wetting" effect on solder which causes the solder to flow smoothly, completely filling the connection. If flux is not used or the metal around the connection is contaminated (dirty) it is almost impossible to have a good solder joint.

Solder bridges are usually caused by using a soldering iron tip that's too large, solder wire that's too large, or trying to rush the job. Use a small spade tip iron (see figure 2). Touch the connection with the flat side of the tip. After the flux bubbles, touch the solder to the opposite side of the connection. Again, don't touch the solder to the iron. The connection is hot enough to melt the solder causing it to flow around the connection. Do not use too much solder. Use a little and watch it flow. Solder is like spice for cooking, don't use too much.

Applying heat for extended periods will cause either or both of the following: the trace or pad will lift from the board or the board material will turn brown. Remove the iron before this happens. One hobbyist counts the bubbles that pop in the solder. He found seven to nine bubbles insured good solder flow without over heating.

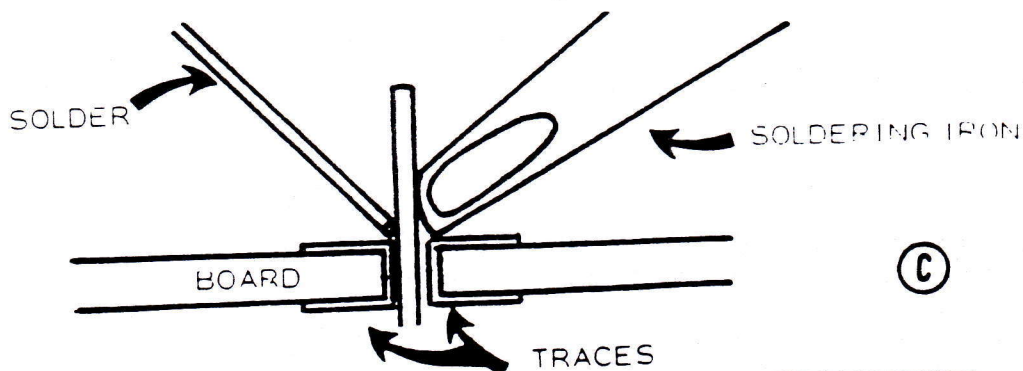


Figure 2.

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The EPM-2 is a memory board designed to interface programmed 2708's or 2716's to the S-100 (WAMECO<sup>TM</sup>) bus (see Tables I and II). Provisions have been made for multiple wait states, memory addressing options and phantom disable. Any multiple of one memory chip can be used in the board and the board start and stop address can be set in 4 K Byte boundaries anywhere in the 65 K Byte memory of your computer. If 4 K Bytes or less, the board can be configured to occupy only the amount of 4 K Bytes in the memory map of your computer. This selection can be increased by 4 K Byte increments until the full 16 K is selected for the 2708 configuration and 32 K for the 2716 configuration. The board is designed to use the single voltage 2716 memory chip.

### Parts List

Schematic Identifier	Quantity	Part
C1, C11, C23, C24, C26, C27, C31	7	22 $\mu$ F 20V Tantalum capacitor
C2-C10, C12-C22, C25, C28, C29, C30	24	.1 $\mu$ F ceramic disc capacitors
R1-R14	14	2.7 K $\Omega$ 1/4 Watt carbon resistors
U1, U32	2	7805, 309T-5, 340T-5
U2, U31	2	74LS138
U3-U10, U14-U21	16	2708 or INTEL 2716
U11	1	7812 or 340T-12
U12	1	7432
U13	1	74LS20
U22	1	7905 or LM320T-5
U23	1	8098 or 74368
U24	1	74LS74
U25, U26	2	7485
U27, U28, U30	3	8097 or 74367
U29	1	7404
S1, S2	2	8 position dip switches
	4	14 pin low profile sockets
	8	16 pin low profile sockets
	16	24 pin low profile sockets
	4	Aham #361 heat sinks
	23	1" jumper wires
	1	insulating washer

### Tools or supplies needed to assemble and test EPM-2

1	Q Tip cotton swab
1	pair needle nose pliers
1	pair diagonal cutting pliers
1	bottle rosin flux
1	tube silicone thermal compound
1	jar solder cleaner
1	roll solder wick
1	Phillips screwdriver
1	small adjustable wrench or socket to fit regulator nut
1	roll (.031" or .040") SN60/40 rosin core solder
1	25 to 40 W soldering iron with small spade tip
1	strong light
1	magnifying glass
1	XACTO knife with number 16 blade
1	multimeter with leads
1	power supply with variable outputs
1	computer w/RAM Memory board



S-100 (WAMECO) BUS DESCRIPTION (continued)

1	+5V	
2	+15V	
3	XRDY	X
4	VI0	X
5	VI1	X
6	VI2	X
7	VI3	X
8	VI4	X
9	VI5	X
10	VI6	X
11	VI7	X
12		
13		
14		
15		
16		
17		
18	STAT DISABLE	X
19	CIC DISABLE	X
20	UNPROTECT	X
21	SS	X
22	ADDR DSBL	X
23	DO DSBL	X
24	02	X
25	01	X
26	PHLDA	X
27	PWAIT	
28	PINTE	
29	A5	
30	A4	
31	A3	
32	A15	
33	A12	
34	A9	
35	DO1	X
36	DO0	X
37	A10	
38	DO4	X
39	DO5	X
40	DO6	X
41	DI2	X
42	DI3	X
43	DI7	X
44	SMI	
45	SOUT	
46	SINP	
47	SMEMR	
48	SHLTA	
49	CLOCK (2MHz)	
50	GND	

Pin MNEMONIC Term.

51	+5V	A	
52	-15V	B	
53	SSW DSB	C	
54	EXT CLR	D	X
55		E	
56		F	
57		H	
58		J	
59		K	
60		L	
61		M	
62		N	
63		P	
64		R	
65		S	
66		T	
67	PHANTOM	U	
68	MWRITE	V	X
69	PS	W	
70	PROTECT	X	X
71	RUN	Y	X
72	PRDY	Z	X
73	PINT	a	X
74	PHOLD	b	X
75	PRESET	c	X
76	PSYNC	d	X
77	PWR	e	X
78	PDBIN	f	X
79	A0	h	
80	A1	j	
81	A2	k	
82	A6	l	
83	A7	m	
84	A8	n	
85	A13	p	
86	A14	r	
87	A11	s	
88	DO2	t	X
89	DO3	u	X
90	DO7	v	X
91	DI4	w	X
92	DI5	x	X
93	DI6	y	X
94	DI1	z	X
95	DI0	AA	X
96	SINTA	AB	
97	SWO	AC	
98	SSTACK	AD	
99	POC	AE	
100	GND	AF	

Pin MNEMONIC Alter. pin desig. Term.

S-100 (WAMECO) BUS DESCRIPTION

Pin #	Mnemonic	Enabled State	Description
1	+8 Volts	NA	Unregulated +8 Volts DC. This voltage should not be less than +8 or greater than +11 volts.
2	+16 Volts	NA	Unregulated +16 Volts DC. This voltage should not be less than +16 or greater than +20 Volts.
3	XRDY	Low	Causes CPU to enter WAIT state when enabled.
4	$\overline{\text{VI0}}$	Low	Vectored Interrupt priority 0
5	$\overline{\text{VI1}}$	Low	Vectored Interrupt priority 1
6	$\overline{\text{VI2}}$	Low	Vectored Interrupt priority 2
7	$\overline{\text{VI3}}$	Low	Vectored Interrupt priority 3
8	$\overline{\text{VI4}}$	Low	Vectored Interrupt priority 4
9	$\overline{\text{VI5}}$	Low	Vectored Interrupt priority 5
10	$\overline{\text{VI6}}$	Low	Vectored Interrupt priority 6
11	$\overline{\text{VI7}}$	Low	Vectored Interrupt priority 7
12	---	NA	Not used
13	---	NA	Not used
14	---	NA	Not used
15	---	NA	Not used
16	---	NA	Not used
17	---	NA	Not used
18	STAT DISABLE	Low	The eight status line buffers on the CPU board enter the high impedance state when enabled.
19	C/C DISABLE	Low	The six command/control line buffers on the CPU board enter the high impedance state when enabled.
20	UNPROTECT	High	Combined with address in an AND gate on a memory board which causes the PROTECT flip-flop to be cleared.
21	SS	High	Indicates the CPU is single stepping.
22	$\overline{\text{ADDR DSBL}}$	Low	The 16 address line buffers on the CPU board enter the high impedance state when enabled.
23	$\overline{\text{DO DSBL}}$	Low	The eight data-out lines on the CPU board enter the high impedance state when enabled.
24	$\emptyset 2$	High	Buffered TTL CPU phase 2 clock.
25	$\emptyset 1$	High	Buffered TTL CPU phase 1 clock.
26	PHLDA	High	CPU board "Hold Acknowledge" to HOLD-H input.
27	PWAIT	High	CPU output showing a WAIT state is occurring.

Figure 3B.



S-100 (WAMECO) BUS DESCRIPTION (Cont.)

Pin #	Mnemonic	Enabled State	Description
28	PINTE	High	CPU output showing that Interrupts are enabled.
29	A5	High	Address Bit 5
30	A4	High	Address Bit 4
31	A3	High	Address Bit 3
32	A15	High	Address Bit 15
33	A12	High	Address Bit 12
34	A9	High	Address Bit 9
35	DO1	High	CPU Data Out Bit 1
36	DO0	High	CPU Data Out Bit 0
37	A10	High	Address Bit 10
38	DO4	High	CPU Data Out Bit 4
39	DO5	High	CPU Data Out Bit 5
40	DO6	High	CPU Data Out Bit 6
41	D12	High	Data In Bit 2 to CPU
42	D13	High	Data In Bit 3 to CPU
43	D17	High	Data In Bit 7 to CPU
44	SM1	High	CPU output indicating it is performing Fetch Instruction.
45	SOUT	High	CPU output showing it is in an output cycle.
46	SINP	High	CPU output showing it is in an input cycle.
47	SMEMR	High	CPU status signal indicating the current cycle is a Memory Read cycle.
48	SHLTA	High	CPU status signal indicating the CPU is halted.
49	CLOCK(2MHz)	Low	A buffered 2 MHz clock for general use.
50	GND	NA	Ground (common)
51	+8 Volts	NA	(Same as pin 1)
52	-16 Volts	NA	Unregulated -16 Volts DC. This voltage should not be greater than -16 or less than -20 Volts.
53	<u>SSW DSB</u>	Low	Sense Switch Disable disables CPU board data input buffers so that CPU can read sense switches.
54	<u>EXT CLR</u>	Low	Front panel generated I/O clear signal.
55	---	NA	Not used
56	---	NA	Not used
57	---	NA	Not used
58	---	NA	Not used
59	---	NA	Not used
60	---	NA	Not used
61	---	NA	Not used
62	---	NA	Not used
63	---	NA	Not used
64	---	NA	Not used
65	---	NA	Not used
66	---	NA	Not used
67	PHANTOM	NA	Used for Memory Bank Selection (or for SOL <sup>®</sup> Systems)

Figure 3B (continued)

S-100 (WAMECO) BUS DESCRIPTION (Cont.)

Pin #	Mnemonic	Enabled State	Description
68	MWRITE	High	CPU output showing Data Out Bus data is to be written into the memory selected by the address lines.
69	$\overline{PS}$	Low	Shows Protect Status of selected memory.
70	PROTECT	High	Combined with address in an AND gate on a memory board which causes the PROTECT flip-flop to be set.
71	RUN	High	Front panel indication that CPU run instruction has been input.
72	PRDY	Low	Causes the CPU to enter the WAIT state when enabled.
73	$\overline{PINT}$	Low	If interrupts have been enabled causes the CPU to enter the Interrupt Acknowledge condition at the conclusion of the current instruction.
74	$\overline{PHOLD}$	Low	CPU input which causes a HOLD status to occur. DMA transfer request signal is $\overline{PHOLD}$ .
75	$\overline{PRESET}$	Low	CPU board system reset signal.
76	PSYNC	High	CPU output showing the start of a new machine cycle. This signal is used on the CPU board to enable the loading of the System Status Latch.
77	$\overline{PWR}$	Low	Indication that data on the Data Out Bus is to be written either to a memory or an I/O device.
78	PDBIN	Low	Indication to the selected memory or I/O device that the CPU expects data on the Data In Bus.
79	A0	High	Address Bit 0
80	A1	High	Address Bit 1
81	A2	High	Address Bit 2
82	A6	High	Address Bit 6
83	A7	High	Address Bit 7
84	A8	High	Address Bit 8
85	A13	High	Address Bit 13
86	A14	High	Address Bit 14
87	A11	High	Address Bit 11
88	DO2	High	CPU Data Out Bit 2
89	DO3	High	CPU Data Out Bit 3
90	DO7	High	CPU Data Out Bit 7
91	DI4	High	Data In Bit 4 to CPU
92	DI5	High	Data In Bit 5 to CPU
93	DI6	High	Data In Bit 6 to CPU

Figure 3B (continued)



S-100 (WAMECO) BUS DESCRIPTION

Pin #	Mnemonic	Enabled State
94	DII	High
95	DIO	High
96	SINTA	High
97	SWO	Low
98	SSTACK	High
99	$\overline{\text{POC}}$	Low
100	GND	NA

NOTE

DO NOT PUT I/O IN SOCKETS AT THIS TIME. THEY WILL BE INSTALLED LATER.

Figure 3B (continued)



## I. Assembly of EPM-2

I-1. Before placing any parts on the board, check the board for any hairline shorts (slivers). All boards have been inspected at least three times before shipping. Still, a good hobbyist checks any board he buys.

I-2. Using a strong light and a magnifying glass, very carefully check all leads on the top of the board ( this is the side marked COMPONENT SIDE). If any slivers are found, carefully cut and scrape them with an XACTO knife. The underside of the board will be checked after assembly.

I-3. Place all the 14, 16, and 24 pin sockets in their positions on the top side of the board.

I-4. After positioning all the sockets in place, check to ensure that a socket is not in the position S1 or S2. Dip switches will not stay in place in a socket. Place a book on top of the sockets, hold the book tight against the board and turn them over so that the underside of the board is up. Press down on the board and solder one pin on each end of each socket. This will ensure the sockets are flat against the board. When the tacking of all sockets is completed, finish soldering all the other pins of the sockets.

### **NOTE**

DO NOT PUT IC'S IN SOCKETS AT THIS TIME. THEY WILL BE INSTALLED LATER.

I-5. Bend the leads on all the resistors ( $2.7K\Omega$  RED, VIOLET, RED) and place in board. Check parts placement drawing (figure 3) for correct locations. Bend the leads of the resistors on the underside of the board to retain them in place until they are soldered. Turn the board over and solder all the resistors. Clip the leads of the resistors flush with the underside of the board with the diagonal pliers.

I-6. Put the leads of C2-C10, C12-C22, C25, C28-C30 ( $.1 \mu F$ ) disc capacitors in the board. Check parts placement drawing (figure 3) for proper locations. Bend the leads of the capacitors to retain them in place until they are soldered. Turn the board over and solder the capacitors. Clip the leads of the capacitors flush with the underside of the board with the diagonal pliers.

I-7. Place C1, C11, C23, C24, C26, C27, C31 ( $22 \mu F$  tantalum) in place. Ensure that the polarities are correct. Check parts placement drawing (figure 3) for correct placement and polarity. Bend the leads of the capacitors to retain them in place until they are soldered. Turn the board over and rest it on books. Solder the capacitors in place. Clip the leads flush with the underside of the board with diagonal pliers.

I-8. Put the eight position dip switches in place. Ensure that switch S1 is installed so that the OFF position is towards the gold fingers of the board and switch S2 is installed so that the OFF position is toward the voltage regulators. Bend the two pins at each end of each switch to retain it in place until it is soldered. Turn the board over and rest it on books as before. Solder the eight position dip switches in place.

COMPONENT SIDE

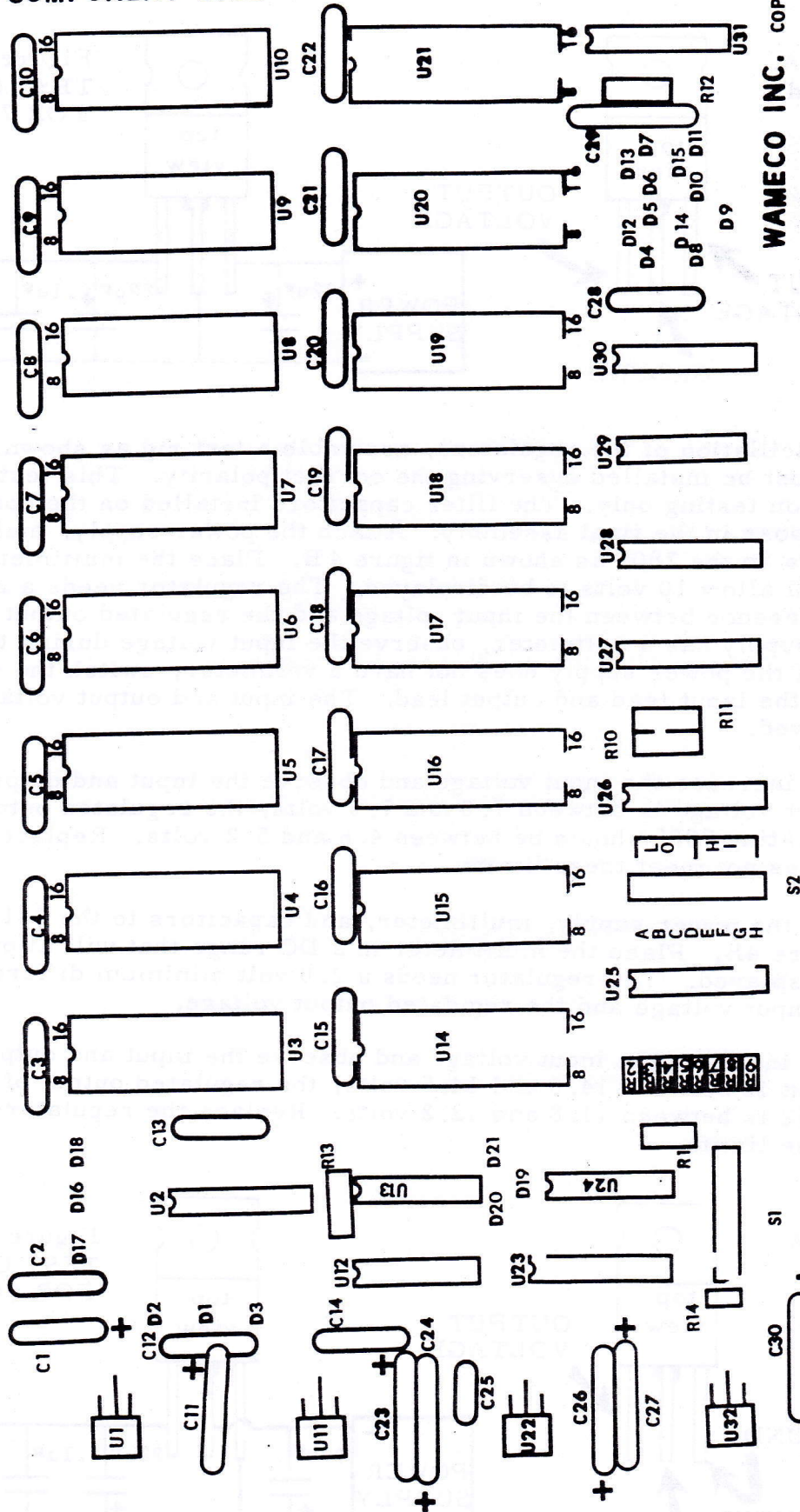
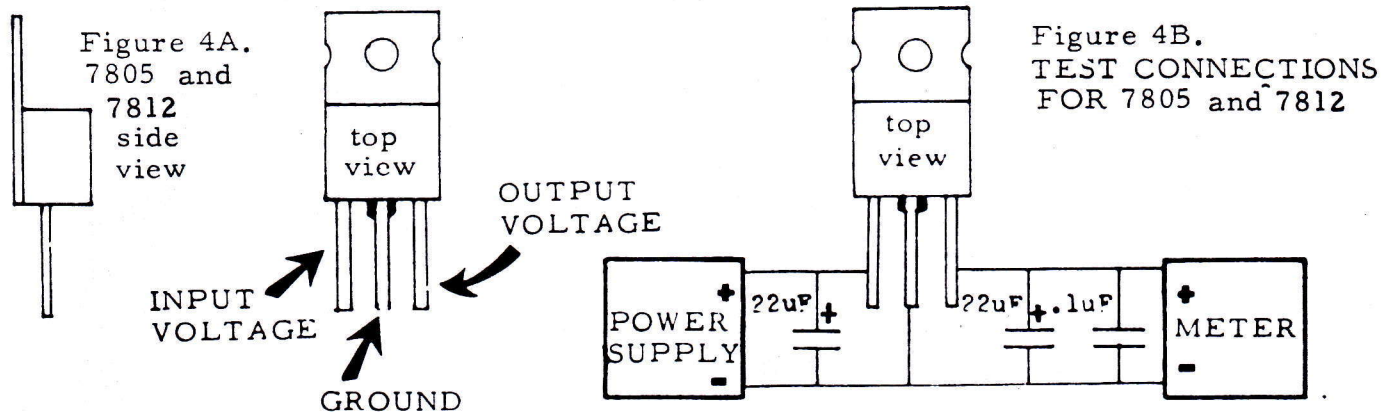


FIGURE 3. EPM-2 PARTS PLACEMENT DIAGRAM



I-9. Before installing the regulators, it is recommended that they be tested for proper voltage regulation.

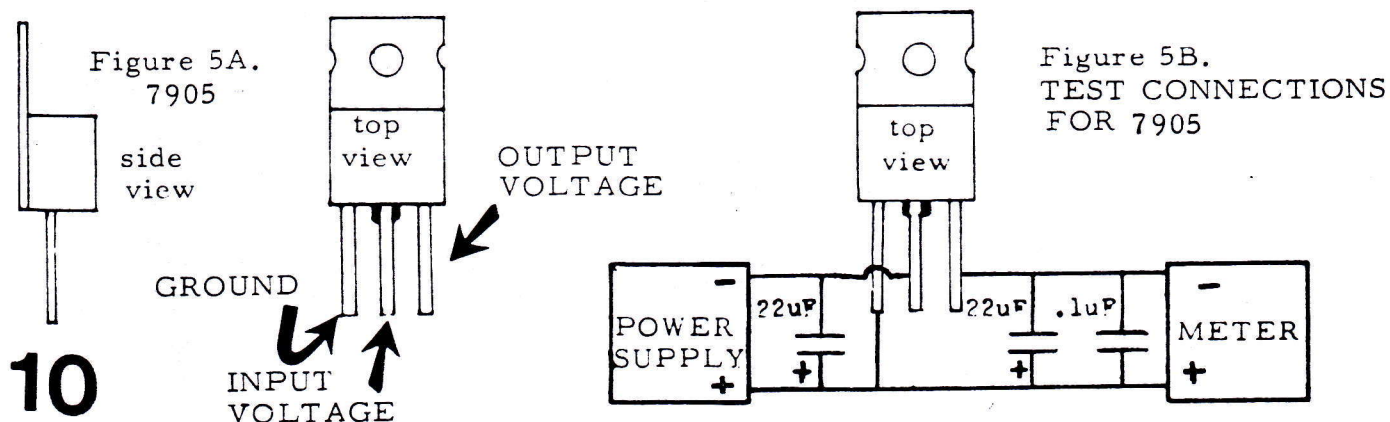


To prevent oscillation of the regulators, assemble a test rig as shown. The capacitors must be installed observing the correct polarity. This test rig is for pre-installation testing only. The filter capacitors installed on the board serve the same purpose in the final assembly. Attach the power supply, multimeter, and capacitors to the 7805 as shown in figure 4B. Place the multimeter in a DC range that will allow 10 volts to be displayed. The regulator needs a 2.0 volt minimum difference between the input voltage and the regulated output voltage. If the power supply has a voltmeter, observe the input voltage during the test using that. If the power supply does not have a voltmeter, switch the + meter lead between the input lead and output lead. The input and output voltages can this be observed.

I-10. Slowly increase the input voltage and observe the input and output voltages. When the input voltage is between 7.0 and 7.5 volts, the regulated output of a properly operating 7805 should be between 4.8 and 5.2 volts. Replace the regulator if it does not meet these limits.

I-11. Attach the power supply, multimeter, and capacitors to the 7812 as shown in figure 4B. Place the multimeter in a DC range that will allow 15 volts to be displayed. The regulator needs a 2.0 volt minimum difference between the input voltage and the regulated output voltage.

I-12. Slowly increase the input voltage and observe the input and output voltages. When the input is between 14.0 and 14.5 volts, the regulated output of a properly operating 7812 is between 11.8 and 12.2 volts. Replace the regulator if it does not meet these limits.





I-13. Attach the power supply, multimeter, and capacitors to the 7905 as shown in figure 5 B. Place the multimeter in a DC range that will allow 10 volts to be displayed. The 7905 needs a 2.0 volt minimum difference between the input and regulated output to work properly. If the power supply does not have a voltmeter, switch the - meter lead between the output and the input lead of the regulator during the test.

I-14. Slowly increase the input voltage and observe the input and output voltages. When the input voltage is between 7.0 and 7.5 volts, the regulated output of a properly operating 7905 should be between 4.5 and 5.5 volts. Replace the regulator if it does not meet these limits.

I-15. When the regulators have been tested as outlined in I-10 through I-14, place the regulators on the board so that the mounting hole of the regulator lines up with the corresponding hole of the EPM-2. Check the parts placement drawing (figure 3) for correct placement of the regulator. Note where the leads of the regulator pass over the connection holes on the EPM-2. Bend the leads of the regulator so that the leads can be inserted into the proper holes. Mount the regulator on the board using a #6 nut and a 5/8" 6-30 screw. Insert a heatsink between the board and the regulator. Solder the leads of the regulator in place.

I-16. Remove the nut and screw from the regulator. Bend the regulator upward and remove the heatsink. Place a moderate amount of thermal compound on the underside of the regulator and heatsink with a cotton swab. Coat all of the area mentioned with an even layer of the thermal compound, reinstall the heatsink, nut and screw. On the 7905's install the insulating washer to isolate the -15V input from ground. Ensure the nut is tight.

I-17. Clean off the flux on the underside of the board with flux cleaner.

## II. Inspection and Testing

II-1. Use a bright light and magnifying glass to inspect all the traces on the underside of the board. If any slivers are found, cut and scrape them with an XACTO knife. Use the solder wick and soldering iron to remove any solder bridges found. Cover the solder bridge with flux and place a clean piece of solder wick on top of the bridge. Place the soldering iron on top of the solder wick and hold until solder is seen flowing up into the solder wick. Remove the iron and wick. Check to see if the bridge has been completely removed. If not, repeat the process until the bridge has been removed. Clean the flux off the board with flux cleaner.

### **NOTE**

AT THIS TIME, NO IC'S HAVE BEEN INSTALLED ON THE BOARD.  
DO NOT INSTALL IC'S ON THE BOARD UNTIL CALLED FOR IN THE  
CHECK OUT PROCEDURE.

II-2. Place the multimeter in the R x 1 scale. Place one probe on the gold finger for pin 1. Place the other probe sequentially on all the other fingers to check for shorts. Repeat this procedure for each pin. There should be only two sets of pins that are shorted; 1 to 51 and 50 to 100. If any other pair of pins are shorted, use a strong light and magnifying glass to locate the solder bridge or silver causing



the short. When the short has been located, correct it as outlined in II-1. If there is no solder bridge or sliver, a component is shorted. Check the EPM-2 schematic (figure 6) to locate the probable component. Lift one lead of the suspected component and recheck between the two fingers that had a bad reading. If the bad reading is now correct, replace the component. If the reading is still bad, continue troubleshooting until the faulty component is located and replaced. Ensure that all components that had a lead lifted have the lead reconnected.

## WARNING

DO NOT INSTALL OR REMOVE ANY BOARD IN COMPUTER WITH POWER ON. DAMAGE TO BOARDS AND COMPUTER MAY RESULT.

II-3. Ensure computer is OFF. Plug EPM-2 into the motherboard. Check that the EPM-2 is correctly plugged in and that the board is fully seated in the connector. Turn the computer power ON and check the outputs of each regulator on the EPM-2. If the regulators do not have output voltages as stated in I-10, I-12, and I-14, turn the computer power OFF and replace the defective regulator. Repeat I-10, I-12, or I-14 as appropriate to check out the new regulator before installing. If the voltage on the regulators are not correct now, check the voltages on the motherboard. If the voltages on the motherboard are incorrect, repair the power supply as needed. If and when the voltages check good, turn the computer power OFF and remove the EPM-2 from the motherboard.

II-4. Select the proper wait state and EPROM configuration on the board by installing the jumpers on the EPM-2 as shown in table III.

II-5. Clean off the flux on the underside of the board with flux cleaner.

II-6. Install all the IC's on the EPM-2. Check parts placement drawing (figure 3) for proper location and correct polarity of IC's.

## CAUTION

ENSURE ALL IC'S ARE INSTALLED CORRECTLY. INCORRECT POLARIZATION OF IC WILL RESULT IN DAMAGE TO IC AND CAUSE SUBSEQUENT TROUBLES TO APPEAR ON THE BOARD.

II-7. The address range of the EPM-2 is set by the start and stop address selected on S2. The minimum range is 4 K Bytes. Select the address range desired using the memory address range select portion of Table III.

II-8. The EPM-2 may be populated one EPROM at a time. The lowest memory address on the board is the top left hand chip U3. The address range increases to the right. The lower row of EPROMs are the higher addresses and also increase to the right. The highest address chip is U21.



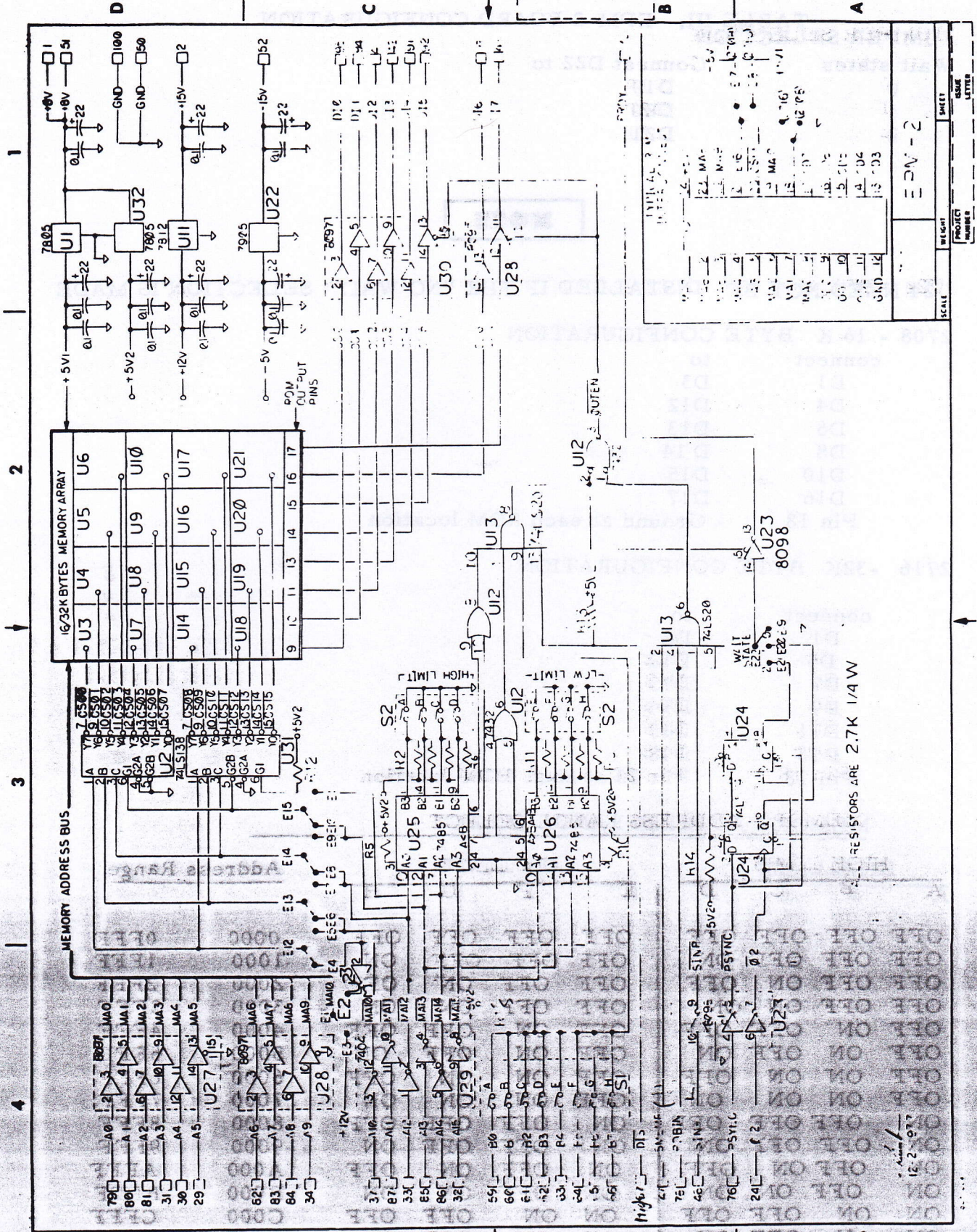


FIGURE 6. EPM-2 SCHEMATIC

406  
 446-3122  
 CNUC



TABLE III. EPM-2 BOARD CONFIGURATION  
 JUMPER SELECTION

Wait states	Connect D22 to
0	D19
1	D20
2	D21

**NOTE**

U24 NEED NOT BE INSTALLED IF THE "NO WAIT" SELECTION IS MADE

2708 - 16 K BYTE CONFIGURATION

connect	to
D1	D3
D4	D12
D6	D13
D8	D14
D10	D15
D16	D17
Pin 18	Ground at each ROM location

2716 - 32K BYTE CONFIGURATION

connect	to
D1	D2
D5	D12
D7	D13
D9	D14
D11	D15
D16	D18
Pin 18	Pin 20 at each ROM location

MEMORY ADDRESS RANGE SELECT -

HIGH LIMIT				LOW LIMIT				Address Range	
A	B	C	D	E	F	G	H		
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0000	0FFF
OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	1000	1FFF
OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	2000	2FFF
OFF	OFF	ON	ON	OFF	OFF	ON	ON	3000	3FFF
OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	4000	4FFF
OFF	ON	OFF	ON	OFF	ON	OFF	ON	5000	5FFF
OFF	ON	ON	OFF	OFF	ON	ON	OFF	6000	6FFF
OFF	ON	ON	ON	OFF	ON	ON	ON	7000	7FFF
ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	8000	8FFF
ON	OFF	OFF	ON	ON	OFF	OFF	ON	9000	9FFF
ON	OFF	ON	OFF	ON	OFF	ON	OFF	A000	AFFF
ON	OFF	ON	ON	ON	OFF	ON	ON	B000	BFFF
ON	ON	OFF	OFF	ON	ON	OFF	OFF	C000	CFFF
ON	ON	OFF	ON	ON	ON	OFF	ON	D000	DFFF
ON	ON	ON	OFF	ON	ON	ON	OFF	E000	EFFF
ON	ON	ON	ON	ON	ON	ON	ON	F000	FFFF



TABLE III EPM-2 BOARD CONFIGURATION CONT.

ADDRESS SELECT REQUIREMENT:

Low Limit Setting  $\leq$  Desired Address Range  $<$  High Limit Setting

**NOTE**

IT IS RECOMMENDED THAT TAPE BE APPLIED OVER THE ERASE WINDOWS OF THE EPROM'S AFTER THEY ARE PROGRAMMED. THERE HAVE BEEN CASES WHERE A GRADUAL ERASURE OCCURRED BECAUSE OF EXPOSURE TO ORDINARY LIGHT.

II-9. Program the EPROM with the program given in figure 7. Install the EPROM in the first location to be tested (U3). The program given for the EPROM will sequentially check all the address and data access lines for the location that the EPROM is inserted in.

**NOTE**

FIGURE 7 DOES NOT CONTAIN THE COMPLETE PROGRAM. EVERY 256 LOCATIONS, THE SOURCE STATEMENTS ARE LOOPED. AT SEQUENCE 293, DB  $\emptyset$  STARTED AND IS INCREMENTED EACH SEQUENCE UP TO SEQUENCE 548 WHICH IS DB 255. THIS IS REPEATED UNTIL ALL THE MEMORY LOCATIONS OF THE EPROM ARE PROGRAMMED.

II-10. Ensure the computer is OFF. Plug the EPM-2 into the motherboard. Check that the EPM-2 is correctly plugged in and that the board is fully seated in the connector.

II-11. Set the address of the RAM board to 00000. Plug the RAM board into the motherboard. Check that the RAM board is correctly plugged in and that the board is fully seated in the connector.

**NOTE**

WHEN POWER IS APPLIED TO AN 8080 SYSTEM, THE MICROPROCESSOR DOES NOT COME UP IN ANY DETERMINABLE MODE. TO CORRECTLY INITIALIZE THE COMPUTER, HOLD THE STOP SWITCH IN STOP AND PUSH THE RESET TO RESET.

II-12. Turn the computer ON. Set the starting address of the EPROM board into the computer and select EXAMINE.

II-13. Enter the most significant Byte of the start address into the data switches (port FF).

II-14. Select RUN. The program will loop at 0H if the test is good.

LOC	OBJ	SEQ	SOURCE STATEMENT
		1	CSEG
0000	210000	2	LXI H, 0
0003	36C3	3	MVI M, 0C3H ;JMP TO ZERO, GOOD TEST
0005	23	4	INX H
0006	AF	5	XRA A
0007	77	6	MOV M, A
0008	23	7	INX H
0009	77	8	MOV M, A
000A	210800	9	LXI H, 8 ;ERROR ADDRESS
000D	36C3	10	MVI M, 0C3H
000F	23	11	INX H
0010	3608	12	MVI M, 8
0012	23	13	INX H
0013	77	14	MOV M, A
0014	DBFF	15	IN 0FFH ;GET START OF MEM TEST
0016	67	16	MOV H, A
0017	C604	17	ADI 4
0019	322200	18	STA 22H ;SAVE END OF TEST ADDRESS
001C	2E26	19	MVI L, 26H
001E	222000	20	SHLD 20H ;SAVE IT
0021	0600	21	MVI B, 1 ;CLEAR COUNTER
0023	EB	22	XCHG
0024	1E3D	23	MVI E, 3DH
0026	1A	24	LOOP: LDAX D
0027	EB	25	XCHG
0028	223000	26	SHLD 30H
002B	EB	27	XCHG
002C	B8	28	CMP B
002D	C20800	29	JNZ 8 ;DOESNT COMPARE, ERROR
0030	13	30	INX D
0031	04	31	INR B
0032	3A2200	32	LDA 22H
0035	BA	33	CMP D
0036	CA0000	34	JZ 0 ;DONE, ALL OK!
0039	2A2000	35	LHLD 20H
003C	E9	36	PCHL ;LOOP BACK
		37	
003D	01	38	DB 1
003E	02	39	DB 2
003F	03	40	DB 3
0040	04	41	DB 4
0041	05	42	DB 5
0042	06	43	DB 6
0043	07	44	DB 7
0044	08	45	DB 8
0045	09	46	DB 9
0046	0A	47	DB 10
0047	0B	48	DB 11
0048	0C	49	DB 12
0049	0D	50	DB 13
004A	0E	51	DB 14
004B	0F	52	DB 15



LOC	HEX	SEQ	SOURCE STATEMENT	LOC	HEX	SEQ	SOURCE STATEMENT
0040	10	53	DB 16	0082	47	108	DB 71
0040	11	54	DB 17	0084	48	109	DB 72
004E	12	55	DB 18	0085	49	110	DB 73
004F	13	56	DB 19	0086	4A	111	DB 74
0050	14	57	DB 20	0087	4B	112	DB 75
0051	15	58	DB 21	0088	4C	113	DB 76
0052	16	59	DB 22	0089	4D	114	DB 77
0053	17	60	DB 23	008A	4E	115	DB 78
0054	18	61	DB 24	008B	4F	116	DB 79
0055	19	62	DB 25	008C	50	117	DB 80
0056	1A	63	DB 26	008D	51	118	DB 81
0057	1B	64	DB 27	008E	52	119	DB 82
0058	1C	65	DB 28	008F	53	120	DB 83
0059	1D	66	DB 29	0090	54	121	DB 84
005A	1E	67	DB 30	0091	55	122	DB 85
005B	1F	68	DB 31	0092	56	123	DB 86
005C	20	69	DB 32	0093	57	124	DB 87
005D	21	70	DB 33	0094	58	125	DB 88
005E	22	71	DB 34	0095	59	126	DB 89
005F	23	72	DB 35	0096	5A	127	DB 90
0060	24	73	DB 36	0097	5B	128	DB 91
0061	25	74	DB 37	0098	5C	129	DB 92
0062	26	75	DB 38	0099	5D	130	DB 93
0063	27	76	DB 39	009A	5E	131	DB 94
0064	28	77	DB 40	009B	5F	132	DB 95
0065	29	78	DB 41	009C	60	133	DB 96
0066	2A	79	DB 42	009D	61	134	DB 97
0067	2B	80	DB 43	009E	62	135	DB 98
0068	2C	81	DB 44	009F	63	136	DB 99
0069	2D	82	DB 45	00A0	64	137	DB 100
006A	2E	83	DB 46	00A1	65	138	DB 101
006B	2F	84	DB 47	00A2	66	139	DB 102
006C	30	85	DB 48	00A3	67	140	DB 103
006D	31	86	DB 49	00A4	68	141	DB 104
006E	32	87	DB 50	00A5	69	142	DB 105
006F	33	88	DB 51	00A6	6A	143	DB 106
0070	34	89	DB 52	00A7	6B	144	DB 107
0071	35	90	DB 53	00A8	6C	145	DB 108
0072	36	91	DB 54	00A9	6D	146	DB 109
0073	37	92	DB 55	00AA	6E	147	DB 110
0074	38	93	DB 56	00AB	6F	148	DB 111
0075	39	94	DB 57	00AC	70	149	DB 112
0076	3A	95	DB 58	00AD	71	150	DB 113
0077	3B	96	DB 59	00AE	72	151	DB 114
0078	3C	97	DB 60	00AF	73	152	DB 115
0079	3D	98	DB 61	00B0	74	153	DB 116
007A	3E	99	DB 62	00B1	75	154	DB 117
007B	3F	100	DB 63	00B2	76	155	DB 118
007C	40	101	DB 64	00B3	77	156	DB 119
007D	41	102	DB 65	00B4	78	157	DB 120
007E	42	103	DB 66	00B5	79	158	DB 121
007F	43	104	DB 67	00B6	7A	159	DB 122
0080	44	105	DB 68	00B7	7B	160	DB 123
0081	45	106	DB 69	00B8	7C	161	DB 124
0082	46	107	DB 70	00B9	7D	162	DB 125

FIGURE 7. EPROM PROGRAM LISTING (Continued)

LOC	OBJ	SEQ	SOURCE STATEMENT	LOC	OBJ	SEQ	SOURCE STATEMENT
00EA	7E	163	DB 126	00F1	B5	218	DB 181
00EB	7F	164	DB 127	00F2	B6	219	DB 182
00EC	80	165	DB 128	00F3	B7	220	DB 183
00ED	81	166	DB 129	00F4	B8	221	DB 184
00EE	82	167	DB 130	00F5	B9	222	DB 185
00EF	83	168	DB 131	00F6	BA	223	DB 186
00F0	84	169	DB 132	00F7	BB	224	DB 187
00F1	85	170	DB 133	00F8	BC	225	DB 188
00F2	86	171	DB 134	00F9	BD	226	DB 189
00F3	87	172	DB 135	00FA	BE	227	DB 190
00F4	88	173	DB 136	00FB	BF	228	DB 191
00F5	89	174	DB 137	00FC	C0	229	DB 192
00F6	8A	175	DB 138	00FD	C1	230	DB 193
00F7	8B	176	DB 139	00FE	C2	231	DB 194
00F8	8C	177	DB 140	00FF	C3	232	DB 195
00F9	8D	178	DB 141	0100	C4	233	DB 196
00FA	8E	179	DB 142	0101	C5	234	DB 197
00FB	8F	180	DB 143	0102	C6	235	DB 198
00FC	90	181	DB 144	0103	C7	236	DB 199
00FD	91	182	DB 145	0104	C8	237	DB 200
00FE	92	183	DB 146	0105	C9	238	DB 201
00FF	93	184	DB 147	0106	CA	239	DB 202
0000	94	185	DB 148	0107	CB	240	DB 203
0001	95	186	DB 149	0108	CC	241	DB 204
0002	96	187	DB 150	0109	CD	242	DB 205
0003	97	188	DB 151	010A	CE	243	DB 206
0004	98	189	DB 152	010B	CF	244	DB 207
0005	99	190	DB 153	010C	D0	245	DB 208
0006	9A	191	DB 154	010D	D1	246	DB 209
0007	9B	192	DB 155	010E	D2	247	DB 210
0008	9C	193	DB 156	010F	D3	248	DB 211
0009	9D	194	DB 157	0110	D4	249	DB 212
000A	9E	195	DB 158	0111	D5	250	DB 213
000B	9F	196	DB 159	0112	D6	251	DB 214
000C	A0	197	DB 160	0113	D7	252	DB 215
000D	A1	198	DB 161	0114	D8	253	DB 216
000E	A2	199	DB 162	0115	D9	254	DB 217
000F	A3	200	DB 163	0116	DA	255	DB 218
00E0	A4	201	DB 164	0117	DB	256	DB 219
00E1	A5	202	DB 165	0118	DC	257	DB 220
00E2	A6	203	DB 166	0119	DD	258	DB 221
00E3	A7	204	DB 167	011A	DE	259	DB 222
00E4	A8	205	DB 168	011B	DF	260	DB 223
00E5	A9	206	DB 169	011C	E0	261	DB 224
00E6	AA	207	DB 170	011D	E1	262	DB 225
00E7	AB	208	DB 171	011E	E2	263	DB 226
00E8	AC	209	DB 172	011F	E3	264	DB 227
00E9	AD	210	DB 173	0120	E4	265	DB 228
00EA	AE	211	DB 174	0121	E5	266	DB 229
00EB	AF	212	DB 175	0122	E6	267	DB 230
00EC	B0	213	DB 176	0123	E7	268	DB 231
00ED	B1	214	DB 177	0124	E8	269	DB 232
00EE	B2	215	DB 178	0125	E9	270	DB 233
00EF	B3	216	DB 179	0126	EA	271	DB 234
00F0	B4	217	DB 180	0127	EB	272	DB 235

FIGURE 7. EPROM PROGRAM LISTING (Continued)



LOC	OBJ	SEQ	SOURCE STATEMENT	LOC	OBJ	SEQ	SOURCE STATEMENT
0128	EC	273	DB 236	015F	23	328	DB 35
0129	ED	274	DB 237	0160	24	329	DB 36
012A	EE	275	DB 238	0161	25	330	DB 37
012B	EF	276	DB 239	0162	26	331	DB 38
012C	FO	277	DB 240	0163	27	332	DB 39
012D	F1	278	DB 241	0164	28	333	DB 40
012E	F2	279	DB 242	0165	29	334	DB 41
012F	F3	280	DB 243	0166	2A	335	DB 42
0130	F4	281	DB 244	0167	2B	336	DB 43
0131	F5	282	DB 245	0168	2C	337	DB 44
0132	F6	283	DB 246	0169	2D	338	DB 45
0133	F7	284	DB 247	016A	2E	339	DB 46
0134	F8	285	DB 248	016B	2F	340	DB 47
0135	F9	286	DB 249	016C	30	341	DB 48
0136	FA	287	DB 250	016D	31	342	DB 49
0137	FB	288	DB 251	016E	32	343	DB 50
0138	FC	289	DB 252	016F	33	344	DB 51
0139	FD	290	DB 253	0170	34	345	DB 52
013A	FE	291	DB 254	0171	35	346	DB 53
013B	FF	292	DB 255	0172	36	347	DB 54
013C	00	293	DB 0	0173	37	348	DB 55
013D	01	294	DB 1	0174	38	349	DB 56
013E	02	295	DB 2	0175	39	350	DB 57
013F	03	296	DB 3	0176	3A	351	DB 58
0140	04	297	DB 4	0177	3B	352	DB 59
0141	05	298	DB 5	0178	3C	353	DB 60
0142	06	299	DB 6	0179	3D	354	DB 61
0143	07	300	DB 7	017A	3E	355	DB 62
0144	08	301	DB 8	017B	3F	356	DB 63
0145	09	302	DB 9	017C	40	357	DB 64
0146	0A	303	DB 10	017D	41	358	DB 65
0147	0B	304	DB 11	017E	42	359	DB 66
0148	0C	305	DB 12	017F	43	360	DB 67
0149	0D	306	DB 13	0180	44	361	DB 68
014A	0E	307	DB 14	0181	45	362	DB 69
014B	0F	308	DB 15	0182	46	363	DB 70
014C	10	309	DB 16	0183	47	364	DB 71
014D	11	310	DB 17	0184	48	365	DB 72
014E	12	311	DB 18	0185	49	366	DB 73
014F	13	312	DB 19	0186	4A	367	DB 74
0150	14	313	DB 20	0187	4B	368	DB 75
0151	15	314	DB 21	0188	4C	369	DB 76
0152	16	315	DB 22	0189	4D	370	DB 77
0153	17	316	DB 23	018A	4E	371	DB 78
0154	18	317	DB 24	018B	4F	372	DB 79
0155	19	318	DB 25	018C	50	373	DB 80
0156	1A	319	DB 26	018D	51	374	DB 81
0157	1B	320	DB 27	018E	52	375	DB 82
0158	1C	321	DB 28	018F	53	376	DB 83
0159	1D	322	DB 29	0190	54	377	DB 84
015A	1E	323	DB 30	0191	55	378	DB 85
015B	1F	324	DB 31	0192	56	379	DB 86
015C	20	325	DB 32	0193	57	380	DB 87
015D	21	326	DB 33	0194	58	381	DB 88
015E	22	327	DB 34	0195	59	382	DB 89

FIGURE 7. EPROM PROGRAM LISTING (Continued)



II-15. The program will loop at 8H if the program tests bad. Location 30H will contain the failing address.

II-16. If the first EPROM location tested good, turn the computer OFF and remove the EPM-2 from the computer. Remove the EPROM from the board and place it in the next higher memory location.

II-17. Increase the starting address by 4 if a 2708 is being used, by 8 if a 2716 is being used.

II-18. Repeat steps II-10. II-12 through II-17 until each memory location has been tested.

### **NOTE**

THE PROGRAM IS WRITTEN FOR TESTING USING A 2708. IF A 2716 IS USED, CHANGE SEQ 17 to ADI 8.

II-19. This test will not test your EPROM'S, it will be assumed that the EPROM you use is a known good unit. If any address fails, use the schematic (figure 6) to determine the probable cause.

II-20. The above instructions are written for a computer with a front panel and capable of having a RAM board being addressed to 00000. If you have a system without a front panel, have your jump to start modified to the various addresses needed to test the board. If your system will not allow you to address usable memory at 00000 the program will have to be modified to change the input addresses to the range allowed by your system.

### III. Operation

III-1. If the board is not to be operated in a memory bank selection mode, all switches on S1 are to be set to OFF.

III-2. If memory bank selection is made, the board will respond IF AND ONLY IF:

- A. The address is within the limits selected by S2.
- B. The CPU has selected a memory bank corresponding to the settings of S1.

III-3. If the board is to be operated in bank select, place the switches of S1 in the desired bank ( see Table IV).

### **CAUTION**

DO NOT HAVE MORE THAN ONE SWITCH OF S1 SELECTED ON AT ANY TIME. MULTIPLE ON SETTINGS WILL CONFUSE THE BOARD.



TABLE IV. BANK SWITCH SETTINGS OF S1

<u>SWITCH</u>								<u>BANK</u>
1	2	3	4	5	6	7	8	
ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0
OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	1
OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	2
OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	3
OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	4
OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	5
OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	6
OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	7

IV. GENERAL

IV -1. The WAMECO INCORPORATED product you have purchased has an unconditional guarantee good for a period of ninety (90) days from date of purchase from your dealer against defects in manufacturing. Upon receipt of the board by WAMECO INCORPORATED, pre-paid freight or mailing, the board will be cheerfully replaced and your shipping charges refunded. The guaranty is limited to replacement of the board with an equivalent board even though the board may be defective through negligence in manufacturing or through other fault.

IV-2. For future reference, a print of the front and back traces of the EPM-2 is shown (see figures 8A and B).

IV-3. We sincerely hope that the EPM-2 will give you long and satisfactory service. If you have any problems with the EPM-2, or if you just want to comment on the board, please write to me personally.

*Norm Walters*

Norm Walters  
 President  
 WAMECO INCORPORATED  
 3107 Laneview Drive  
 San Jose, Ca. 95132

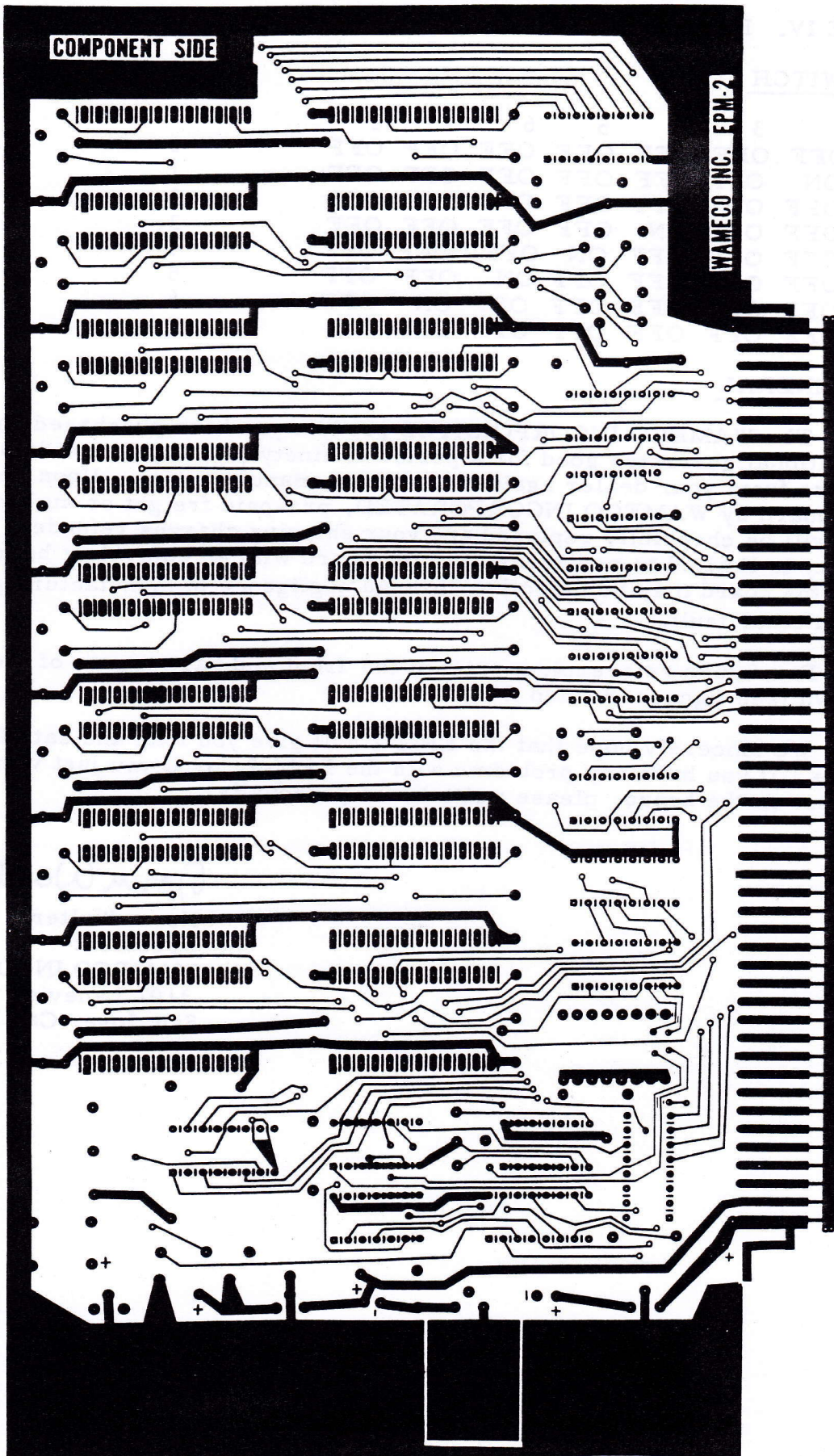


FIGURE 8A. COMPONENT SIDE OF EPM-2



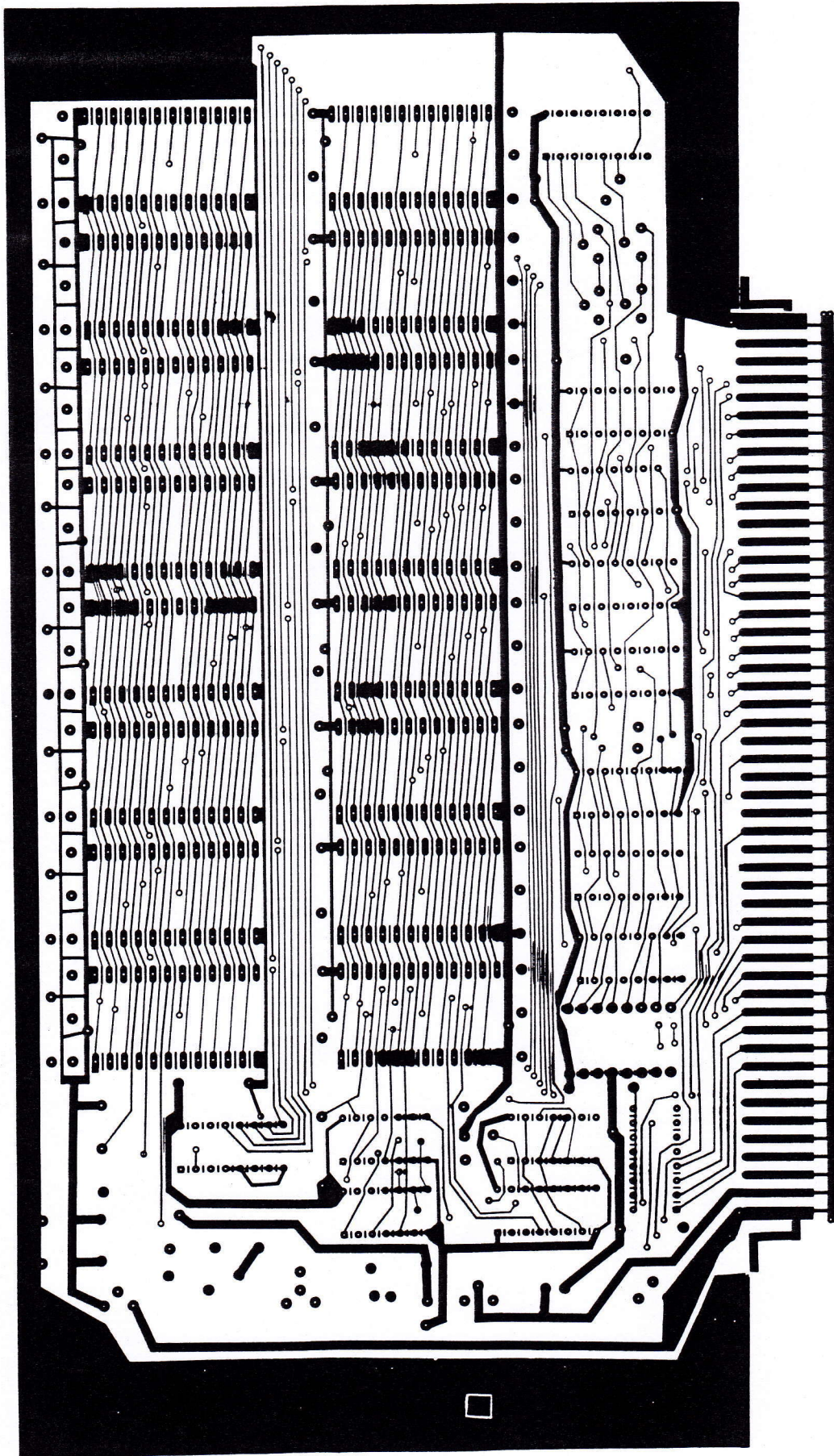


FIGURE 8B. TRACE SIDE OF EPM-2