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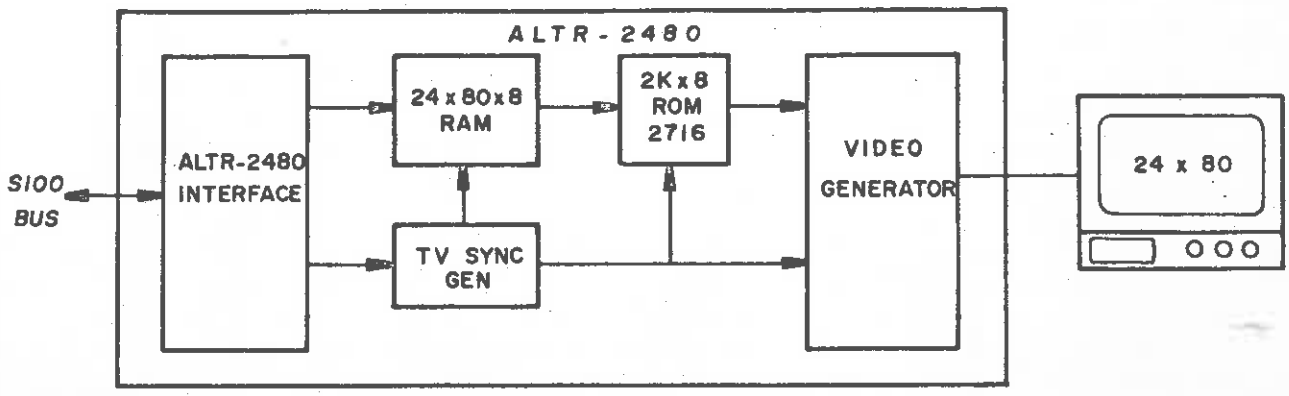
ALTR-2480

MTX TV CRT CONTROLLER FAMILY — ALPHANUMERIC DISPLAY



The ALTR-2480 is a unique single board video interface between S100 type computers and a TV monitor. The board allows S100 users to add a video display to their computer at a very low cost. The ALTR-2480 incorporates a revolutionary display memory design which is completely transparent. Alphanumeric video display boards made by virtually all other manufacturers suffer from interference or streaking when the board is accessed. This occurs because the display memory must be accessed by both the computer and sync generator. The standard solution is to access the card during blanking or to use DMA. Both approaches add complexity and drastically reduce CPU throughout. The Matrox transparent memory is a revolutionary new solution to the classic problem. It is not necessary to wait for blanks, no DMA is used, the CPU operates at full speed, and there is no streaking on the screen no matter how often you access the board.

* Plugs directly in S100 bus
* Upper/lower case/graphics
* 24 lines x 80 characters or 2 pages of 24 x 40 characters
* Byte mapped (4K x 8)
* Built-in R/W refresh memory
* User programmable character generator (2716 EPROM)
* External/internal sync
* Normal/inverse/blink control
* Drives TV monitor directly
* 500 nsec access time
* Single 8V, .8A power supply (unregulated)
* Can be combined with ALT-256 or ALT-512 graphics
* Software package available.
* Full software control

1.0 SPECIFICATIONS FOR ALTR-2480 DISPLAY INTERFACE:

INTRODUCTION: The ALTR-2480 provides an alphanumeric video interface between an S100 bus microcomputer and a TV monitor. It outputs the industry standard 24 line x 80 character display which is invaluable for professional applications such as intelligent CRT terminals and work processors. The ALTR-2480 is compatible with the ALT-256 or ALT-512 graphics interface permitting a powerful combined alphanumeric/graphic display.

DISPLAY FORMAT: 24 lines x 80 character, or 2 pages of 24 x 40 characters.

ADDRESSING: Matrox VRAM organization. Each character position on the screen is equivalent to a memory location (byte). The content of the memory location (byte) determines the character to be displayed. The card occupies 4K bytes of RAM address space. On board jumpers permit address positioning.

REFRESH MEMORY: Built-in on the card (2K x 8 RAM). 500 nsec access.

BUS: S100 bus plug-in.

CHARACTER GENERATOR: Upper and lower case, limited graphics, 128 different characters inside 6 x 10 or 8 x 10 dot matrix. The character generator is a 2K x 8 (2716 EPROM) programmed by Matrox. Custom made fonts can be easily incorporated by programming your own 2716 EPROM.

CURSOR: Any character can be normal intensity, inverse video or blink under software control.

TV STANDARD: American standard (60 Hz), non-interlaced. European standard (50 Hz) non-interlaced. ALTR-2480 will work with any standard TV monitor or modified TV set (10 mHz bandwidth).

OUTPUTS: Composite video; 75 Ohm, x-tal controlled, TTL video, horizontal and vertical sync and blank outputs.

REMOTE DISPLAY: 75 Ohm cable, up to 500 feet, multiple monitors up to 10 TV's.

GRAPHICS: Limited graphics capability built-in. For full graphics, add a graphics ALT-256 board. Both boards can be synchronized together by a simple 4 wire connection.

DIMENSIONS: Standard S100 card size: X 100 pin connector.

DOCUMENTATION: 20 page manual, complete description, schematics.

WARRANTY: 90 days parts and labor.

ORDERING: Available directly from Matrox Electronics Systems Limited, Montreal, Quebec.

2.0 FUNCTIONAL DESCRIPTION:

The ALTR-2480 video interface ram board provides all circuitry required to generate an alphanumeric 24 x 80 character display. The board has all TV timing, I/O circuits, and revolutionary transparent refresh memory built-in. To the 8080A CPU, the ALTR-2480 looks like a static random access memory. It is directly connected to the CPU address and data bus. Each character position on the screen is equivalent to a memory location. It can be written into and read out the same way as any other RAM in the microprocessor address space.

This Matrox video RAM organization allows the programmer to use all 8080A memory reference instructions to manipulate data on the display. This powerful feature can significantly simplify display drivers and save valuable CPU time.

3.0 DISPLAY ADDRESSES:

The ALTR-2480 has a special organization designed to minimize on-board memory while simplifying software. Figure 1 shows this organization. Address lines AØ-A6 are for column addressing, A7-A11 are for row addressing. A12-A15 are the jumper programmable address boundry. The 12 address lines (AØ-A11) of the ALTR-2480 occupy a block of 4K bytes of memory space. Note that only 2K bytes of active memory are used in the VRAM. The seven lines (AØ-A6) used for column addressing could theoretically address 128 locations. Only the first 80 column locations contain active memory. Note that the separate row and column address lines make it easier to calculate the address of a particular location on the screen.

The ALTR-2480 can be configured as a 24 line by 40 character display using appropriate jumpers. In this configuration, the 4K memory has two 2K pages, out of which only one is displayed. (See Figure 2). The first page has address bit AØ always Ø. The second page has AØ always 1. Both pages can be accessed randomly. The ALTR-2480 will display the page selected by bit 1 of the control register.

In addition to the displayed locations, there are two write only control registers. A 2-bit logic video control register and a 1-bit bank select register. The logic video control register is addressed by writing to any location between columns 80 and 95, while the bank select register is addressed by writing to any location between columns 96 and 111.

(Caution: Locations between columns 112 and 127 address BOTH registers simultaneously, and writing to these locations should be avoided unless the programmer is certain of the data being written and is aware of the action that will result.

NOTE: Boards with an issue level below three do not have the bank select option and the video control register on these boards is addressed between columns 79 and 127.

3.1 LOGIC VIDEO CONTROL REGISTER:

D7	D6	D5	D4	D3	D2	D1	DØ
						V1	VØ

Address: Between columns 80 to 95. This is equivalent to Hex addresses SX5Ø to SX5F
or SXDØ to SXDF
where X = any hex digit
and S = most significant base address digit as strapped in S4.

VØ = Ø : Display blanked (Screen black)
Logic Video (S2 Pin 4) low.
VØ = 1 : Display and logic video enabled.
V1 = Ø : Page Ø displayed (odd column addresses)
V1 = 1 : Page 1 displayed (even column addresses)
- This bit is only effective in 24 x 40 display mode, and has no effect in 24 x 80 mode.

These two options are separately enabled or disabled by wire jumpers on the board.

3.2 BANK SELECT REGISTER:

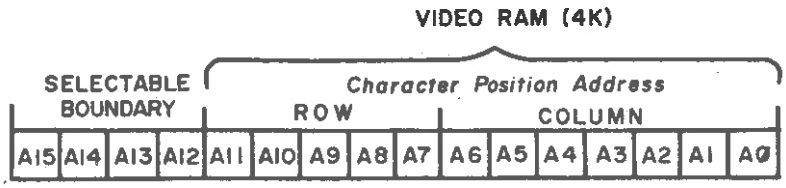
This option allows the use of up to eight ALTR-2480 boards residing in the same address space of the system. In a multiple board system, normal operation requires that each board be strapped to a different data bit using jumper BSØ to BS7. Writing to the bank select locations accesses the bank select registers of all boards simultaneously. This allows the use of a single write instruction to alter the configuration. When set to 1, this register enables the board and when set to Ø, disables it. Disabling a board means that access to the display locations and video control register is inhibited. The bank select register is never inhibited by software commands and the display itself is not affected. Several boards may be enabled at one time, if for example, one wants to write the same information to all of them. Reading from several boards having different data must be avoided, however, as this would cause conflicts on the data bus.

D7	D6	D5	D4	D3	D2	D1	DØ
B7	B6	B5	B4	B3	B2	B1	BØ

Address: Between columns 96 to 111. This is equivalent to Hex addresses SX6Ø to SX6F
or SXEØ to SXEF
where X = any hex digit
and S = most significant base address digis as strapped in S4.

BØ= Ø : Disables board which has jumper BSØ installed.
BØ= 1 : Enables board, which has jumper BSØ installed.

B1 : Enables/disables board with jumper BS1
B2 : Enables/disables board with jumper BS2
B3 : Enables/disables board with jumper BS3
B4 : Enables/disables board with jumper BS4
B5 : Enables/disables board with jumper BS5
B6 : Enables/disables board with jumper BS6
B7 : Enables/disables board with jumper BS7



NOTE: Column addresses 80-127 and row addresses 24-31 are ignored by VRAM.

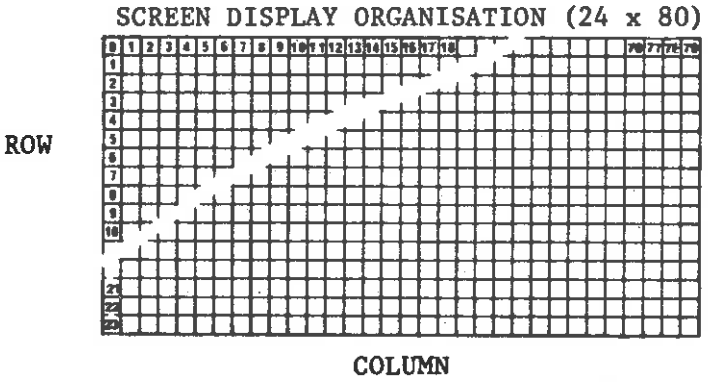


Figure 1 - ADDRESSING THE ALTR-2480 FOR A 24 x 80 ORGANISATION

4.0 THEORY OF OPERATION:

The ALTR-2480 has four major blocks: the TV sync generator, scanning circuitry, video generator and interface and refresh memory. The sync generator is formed of X-tal oscillator A25 and a divider chain A1, 2, 3, 4, 5. This divider chain produces all timing signals for the memory scanning as well as horizontal and vertical sync. The TV sync generator can be programmed for the European or American TV standard.

The scanning circuitry consists of multiplexers A16, 17, 18 and address stearing logic A19, 24, 29.

The video generator consists of an EPROM character generator A11, shift register A13 and associated electronics A7, 12, 28.

Horizontal sync is decoded at the output of A10-6 and vertical sync is decoded at the output of A28-3.

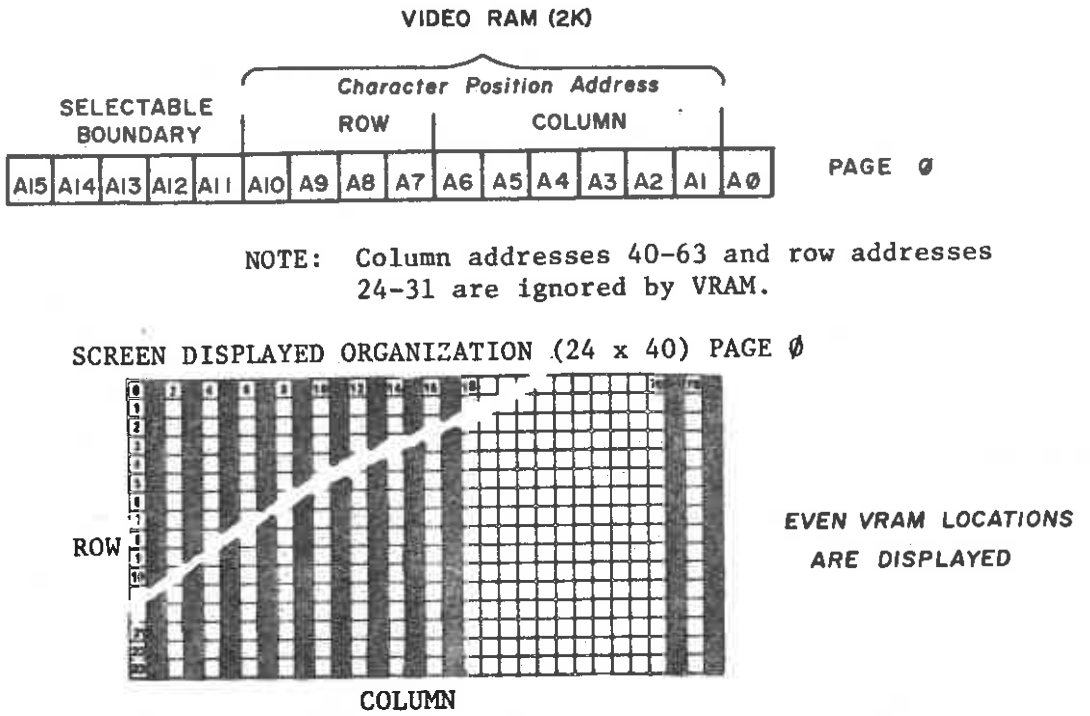
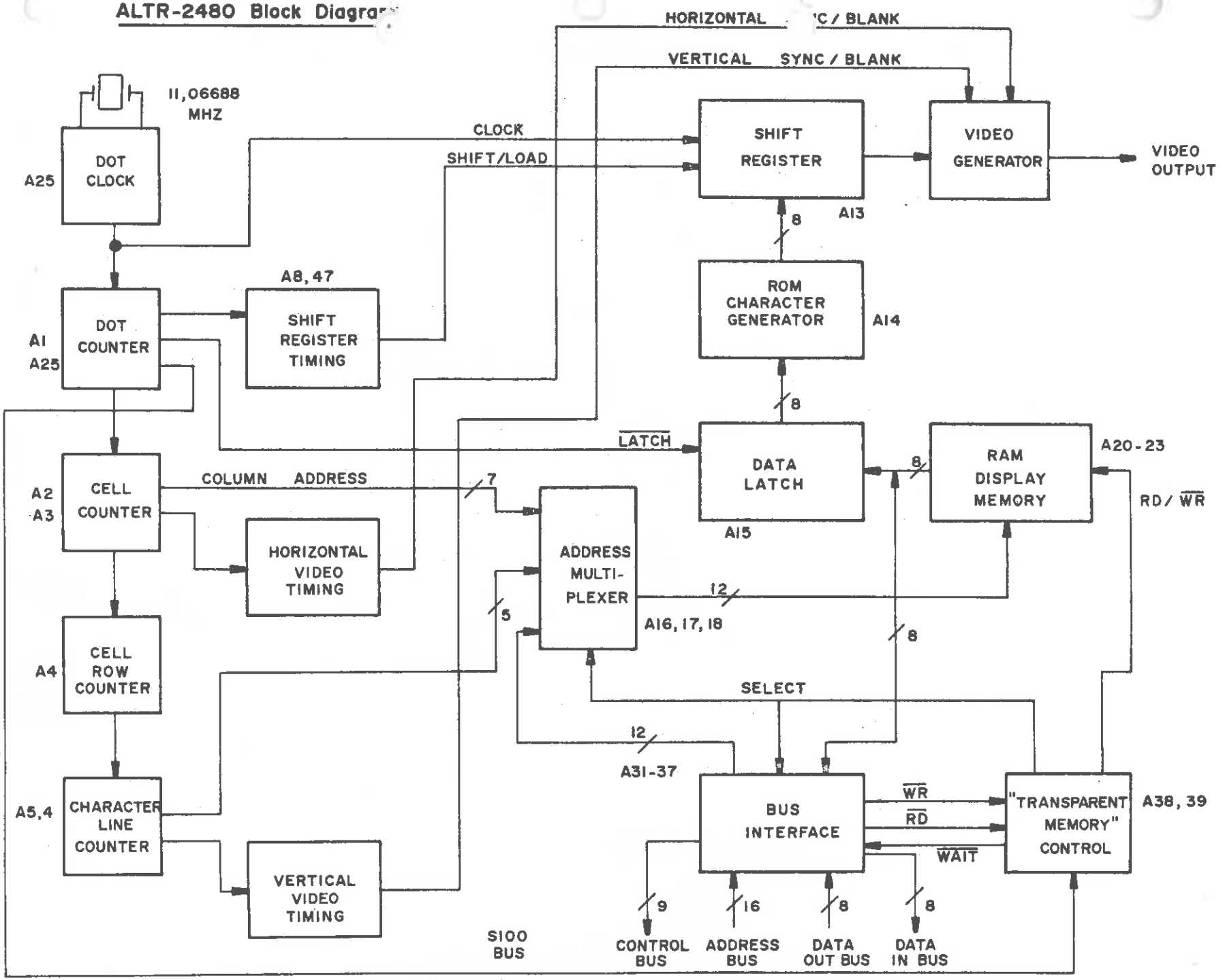


FIGURE 2 - ADDRESSING THE ALTR-2480 FOR A DUAL 24 x 40 ORGANIZATION

ALTR-2480 Block Diagram



4.0 THEORY OF OPERATION: (Cont'd)

The refresh memory A2Ø-23 consists of 4 4K RAM's (2114's) which are organized as a 4K x 8 RAM. However, since the 24 x 80 display uses 1920 locations, only 2K x 8 of RAM is used. The remaining locations (columns from 80 to 127 and rows from 24 to 31) are empty. Stearing logic(A19, 24,and 29)maps the 4K input address lines to 2K memory. The interlaced circuitry consists of A34, 38, 39. This circuitry is responsible for the transparent memory feature.

5.0 PROGRAMMABLE OPTIONS:

The ALTR-2480 can be user programmed (by jumpers) for several configurations. The following parameters are user programmable:

5.1 ADDRESS MAPPING:

The ALTR-2480 occupies 4K of word locations (4K x 8 bytes). This 4K can be positioned anywhere in the address space by selecting chip select lines. This is done by decoding A12-A15 address lines. (Socket S1).

ADDRESS BIT	JUMPER ACROSS (for Ø)	JUMPER ACROSS (for 1)
A12	8 - 9	7 - 10
A13	6 - 11	5 - 12
A14	4 - 13	3 - 14
A15	2 - 15	1 - 16

5.2 TV STANDARD:

The ALTR-2480 can be programmed for American standard (60 Hz) refresh rate or European standard (50 Hz) by jumpers (socket S4 and S5). No x-tal change is required.

Jumpers in:

American Standard:	1-16;	3-14;	5-12;	7-10;	1-16(S5)	(E std. jumpers out)
European Standard:	2-15;	4-13;	6-11;	8- 9;	2-15(S5)	(A std. jumpers out)

5.3 CELL SIZE:

For cell size, selection jumpers are (S3 socket)

A; 6 x 10 cell 1-16, 3-14, 5-12, 7-10 (8 x 10 jumpers out). X-tal is 11.06688 MHz.
B; 8 x 10 cell 2-15, 4-13, 6-11, 8- 9 (6 x 10 jumpers out). X-tal is 14.75584 MHz.

5.4 DISPLAY FORMAT:

For display format, selection jumpers are:

24 x 80 format; in W4, W6, W8 (24 x 40 jumpers out).
24 x 40 format; in W5, W7, W9 (24 x 80 jumpers out).
(Page selection is made by BIT 1 of Control Register).

5.5A Logic Video Control

To enable or disable this option, jumpers are:
Logic video control ENABLE W1Ø in, W11 out.
Logic video control DISABLE W11 in, W1Ø out.

5.5B Bank Select

Bank select option enabled ~~W14~~ W17 out, ~~W15~~ W18 in.
Bank select option disabled ~~W14~~ W17 in, ~~W15~~ W18 out.

Bank Select Jumpers BSØ to BS7

If the bank select option is enabled, then one of the jumpers, BSØ to BS7 must be installed. This jumper determines the register bit to which this board will respond.

5.6 Interlaced Memory (Transparent Memory)

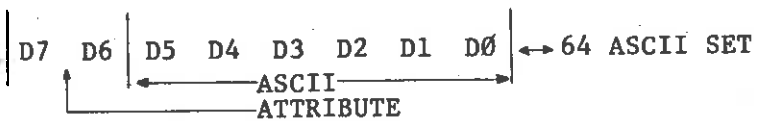
An interlaced memory accessing is possible on the ALTR-2480 boards. This mode can be enabled or disabled by the two jumpers W2, W3.

Interlaced memory: W3 in, W2 out (use fast memories 2114-2).
Non-interlaced memory: W2 in, W3 out (use normal 2114 memories).

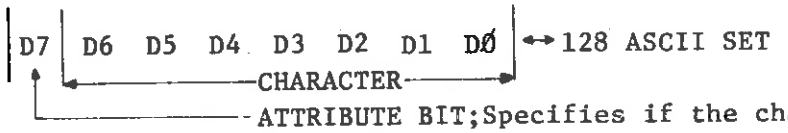
5.7 Display Data Bus Format

As described in Section 3, each memory location in the ALTR-2480 corresponds to a particular character location on the screen. The contents of the 8-bit byte will determine what is seen at the corresponding screen position. The 8-bit byte is partitioned as described below. The least significant 7 bits selects the character to be displayed according to the character generator table. The most significant bit D7 determines if the character attribute is on or off. D7-1 is attribute on, D7-Ø is attribute off. The attribute can be programmed to be inverse, blink or both as described below.

ATTRIBUTE	S5 JUMPERS (+ = IN)						
	3-14	4-13	5-12	6-11	7-10	W-12	W-13
128 ASCII set (D7 disable)	+			+		+	
128 ASCII set (D7 = Ø normal, 1 blink)	+				+	+	
128 ASCII set (D7 = Ø normal, 1 inverse)		+		+		+	
128 ASCII set (D7 = Ø normal, 1 inverse blink)		+			+	+	
64 ASCII set (D7, D6; D5-DØ ASCII)			+		+		+



D7	D6	ATTRIBUTE
0	0	Normal
0	1	Inverse
1	0	Blink
1	1	Blink Inv.



5.8 8080/Z80 (PV Selector)

If the board is used with a 8080 CPU jumper W15 IN W16 OUT
Z80 CPU jumper W16 IN W15 OUT

6.0 EPROM CHARACTER GENERATOR:

The Matrox ALTR-2480 uses an EPROM character generator. This permits easy modifications of the character set. The following is information that permits the user to custom program his own character font.

The ALTR-2480 divides up the screen into an array of 24 lines by 80 characters (See figure 1). Each character position is called a cell and is itself composed of a dot matrix. The ALTR-2480 can have either a 6 x 10 or 8 x 10 dot matrix. The contents of the dot matrix are programmed into the character generator EPROM. Figure 3 shows an example of the character dot matrix for the letter B. The 8 EPROM data outputs contain a horizontal slice through the characters. The EPROM address lines are divided into two groups: four lines are used for row selection, seven lines are used for selecting one of 128 characters.

The standard character generator supplied with the ALTR-2480 contains the full ASCII alphabet plus lower case characters, and 32 special graphics characters. The font is designed for a 6 x 10 cell. Row Ø is normally blank to allow for a vertical space between lines of characters. Rows 8 and 9 are for the descenders of lower case characters. Output Ø8 is normally blank to allow for intercharacter spacing along a line. Outputs 1 and 2 are not visible when the ALTR-2480 is set up for a 6 x 10 cell. Note that the graphic characters utilize all dots including those normally reserved for spaces to allow for drawing continous lines.

EPROM PIN ASSIGNMENTS

	PIN	FUNCTION
01	9	Character outputs which form a horizontal slice through the character.
02	10	
03	11	
04	13	
05	14	
06	15	
07	16	
08	17	
A0	8	Row Select 0 Select one of 10
A1	7	Row Select 1 horizontal slices
A2	6	Row Select 2 through character
A10	T120/Intel 19	Row Select 3 cell.
A3	5	DO LSB
A4	4	D1 Selects one of 128
A5	3	D2 characters from the
A6	2	D3 character generator.
A7	1	D4 These lines are con-
A8	23	D5 nected to the data bus
A9	22	D6 MSB lines indicated.

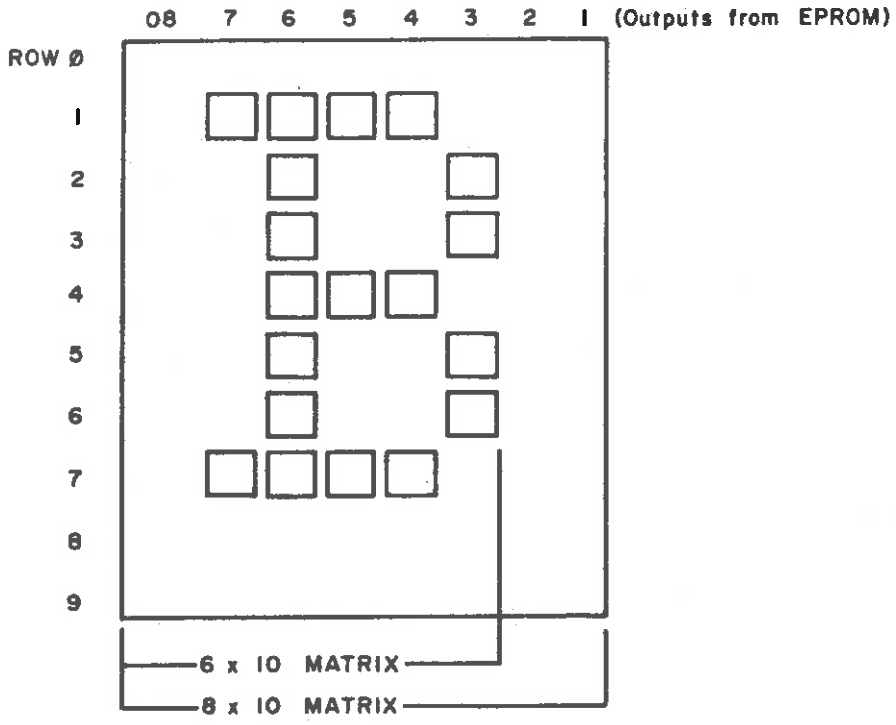
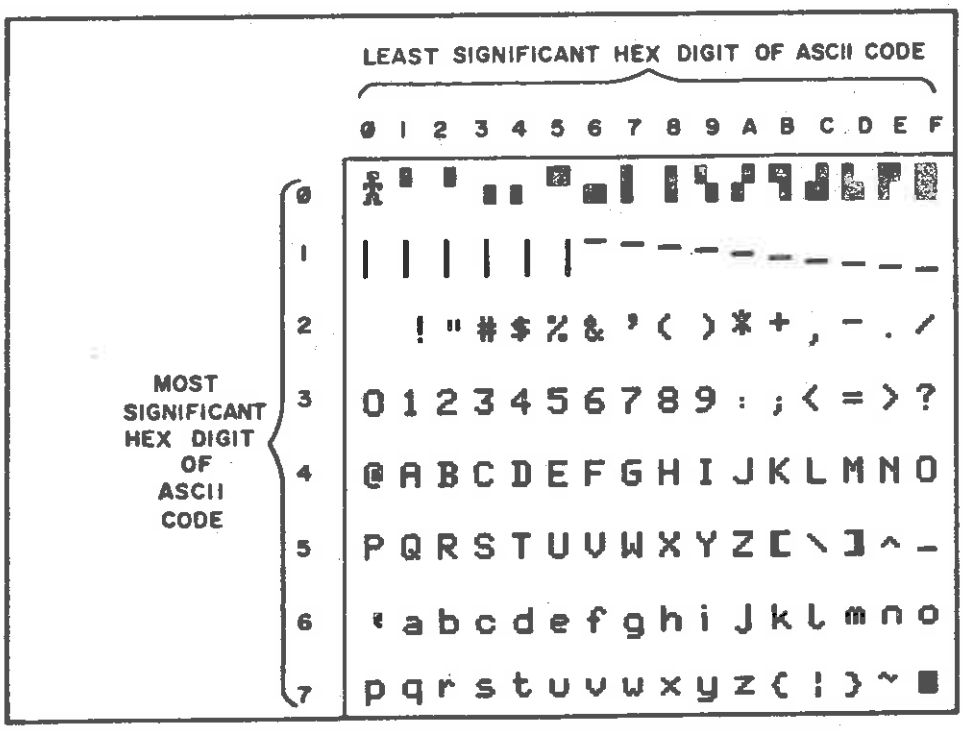


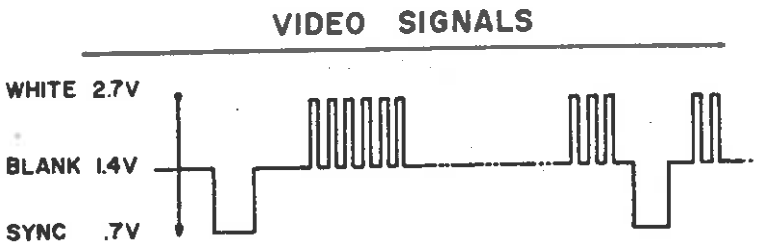
Figure 3 - 7 BIT CODE FOR LETTER "B" IS 1000010



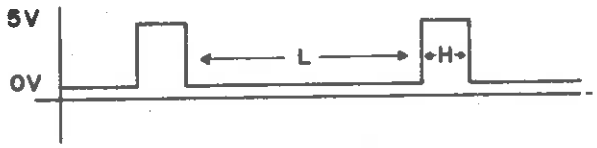
MCH - 001 CHARACTER FONT

7.0 VIDEO SIGNALS (S2 Socket)

The following table gives timing information for the video signals which are present on Socket 2.



COMPOSITE VIDEO SIGNAL. OUTPUT IMPEDANCE 75 Ohms. SHORT CIRCUIT PROTECTION BUILT IN.
PIN V-16



SIGNAL	FREQ.	HIGH	LOW	STD	S2 PIN NO.
SH HORIZONTAL SYNC	15.8 kHz	4.3 us	59. us	AS	14
	15.8 kHz	4.3 us	59. us	ES	
SV VERTICAL SYNC	60 Hz	255 us	16.4 ms	AS	13
	50.2 Hz	255 us	19.7 ms	ES	
$\overline{BH}$ BLANK HORIZONTAL	15.8 kHz	43 us	20 us	AS	12
	15.8 kHz	43 us	20 us	ES	
$\overline{BV}$ BLANK VERTICAL	60 Hz	15.3 ms	1.4 ms	AS	11
	50.2 Hz	15.2 ms	4.7 ms	ES	
DTC DOT CLOCK	11.06688 mHz			AS	1
	11.06688 mHz				

7.1 PINOUTS FOR S4 VIDEO EXPANSION SOCKET:

PIN	NAME	DESCRIPTION
1	DTC	Dot clock (bi-directional)
2	HR	Horizontal reset (bi-directional)
3	VR	Vertical reset (bi-directional)
4	GC	Graphic clock ($\frac{1}{2}$ dot clock)**
5	CSYNC	Composite sync
6	+5V	
7	HR	Horizontal reset (output)**
8	GND	Ground
9	LVID	Logic video (TTL level)
10		
11	VB	Vertical Blank
12	HB	Horizontal Blank
13	SV	Vertical sync
14	SH	Horizontal sync
15	ES	External sync
16	CVDO	Composite video

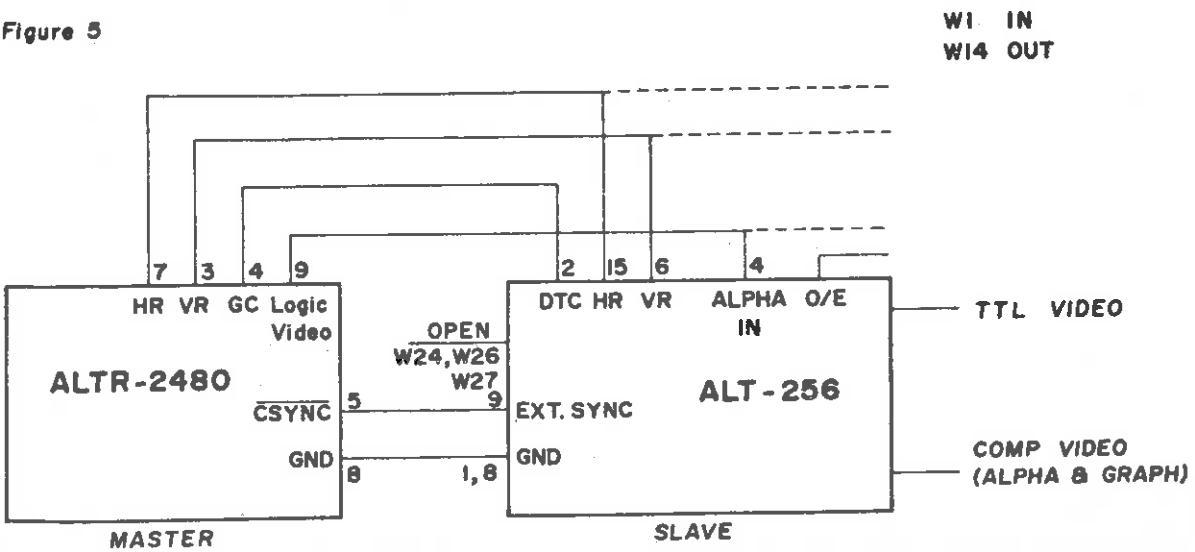
* Composite video is also available for RF connector socket.
** Driving signals for ALT-256 slave boards (old model).

8.0 COMBINING ALTR-2480 AND ALT-256 GRAPHICS BOARDS:

The ALTR-2480 and ALT-256 display cards are directly compatible with one another. This powerful feature permits generation of a combined alpha-numeric/graphics display with no extra hardware. Multiple ALT-256 cards can also be slaved to a single ALTR-2480 master for color/grey scale applications.

Figure 5 shows how the ALTR-2480 and ALT-256 cards are connected together. The connection is accomplished via 16 pin DIP plugs on each card. Some jumpers must be altered on the ALT-256. The combined composite video output is taken from the ALT-256 output.

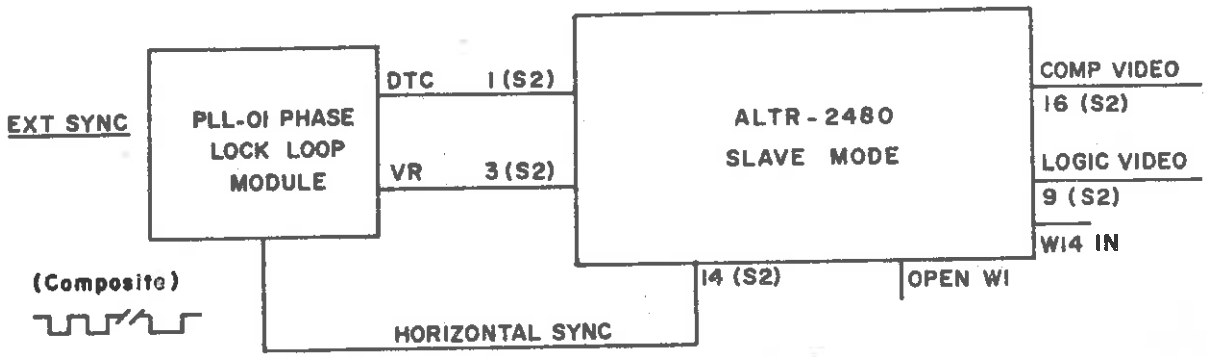
Figure 5



9.0 EXTERNAL SYNC MODE:

The ALTR-2480 can be synchronized to an external sync source such as a TV camera or master sync generator in a TV studio for video mixing or similar function.

This is accomplished by forcing the ALTR-2480 into slave mode and adding the PLL-01 module. (Can be ordered from Matrox). PLL-01 is a phase lock loop which will lock on external sync source and generate dot clock and vertical reset for ALTR-2480.



The ALTR-2480 is forced to slave mode by taking out jumper W1 and putting in jumper W14, and disconnecting (cutting) pin 8 of A25.

10.0 MAINTENANCE AND WARRANTY:

The ALTR-2480 is a fairly complex card and to understand its operation requires extensive knowledge of TV scanning, static memories and hardware. The complete circuit and assembly schematics are supplied to allow a competent user to troubleshoot the board if necessary. However, each board is fully tested, assembled and burned in for 48 hours before shipping to ensure reliability. In case of trouble, a warranty is provided.

Matrox products are warranted against defects in materials and workmanship for a period of three months from date of delivery. We will repair or replace products which prove defective during the warranty period, provided they are returned to Matrox Electronic Systems Limited. No other warranty is expressed or implied. We are not liable for consequential damages.

Non-warranty repairs are billed at a minimum of $50 and according to time and materials required.

11.0 SCHEMATICS TABLES AND OTHER DATA:

11.1 PIN ASSIGNMENT TABLE ALTR-2480:

The following table gives the pin assignments for the ALTR-2480 card and a brief definition of the function of each connection.

11.1 PIN ASSIGNMENT TABLE ALTR-2480:

ALTR-2480 I/O SIGNAL SUMMARY

SIGNAL	PIN NO.	DEFINITION
D1Ø	95	Data input lines
D11	94	
D12	41	
D13	42	
D14	91	
D15	92	
D16	93	
D17	43	
D0Ø	36	Data output lines
D01	35	
D02	88	
D03	89	
D04	38	
D05	39	
D06	40	
D07	90	
AØ	79	Address Lines
A1	80	
A2	81	
A3	31	
A4	30	
A5	29	
A6	82	
A7	83	
A8	84	
A9	34	
A1Ø	37	
A11	87	
A12	33	
A13	85	
A14	86	
A15	32	
SOUT	45	Status output signals which indicates that the address bus contains the address of an output device and the data bus will contain the output when $\overline{PWR}$ is active.
SINP	46	Status output signals which indicates that the address bus contains the address of an input device and the input data should be placed on the data bus when PDWIN is active.
SMEMR	47	Status output signals which indicates that the data bus will be used for memory read data

11.1 PIN ASSIGNMENT TABLE ALTR-2480 (Cont'd)

SIGNAL	PIN NO.	DEFINITION
PDBIN	78	Processor control output signal indicates to external circuits that the data bus is in the input mode.
MWRITE	68	From the front panel indicates that the current data on the data out bus is to be written into the memory location currently on the address bus.
$\overline{\text{PWR}}$	77	Processor control output used for memory write or I/O output control; data on the data bus is stable while the $\overline{\text{PWR}}$ is active.
PRDY	72	Processor command/control input that controls the run state.
SINTA	96	Status output signal to acknowledge signal for interrupt request.

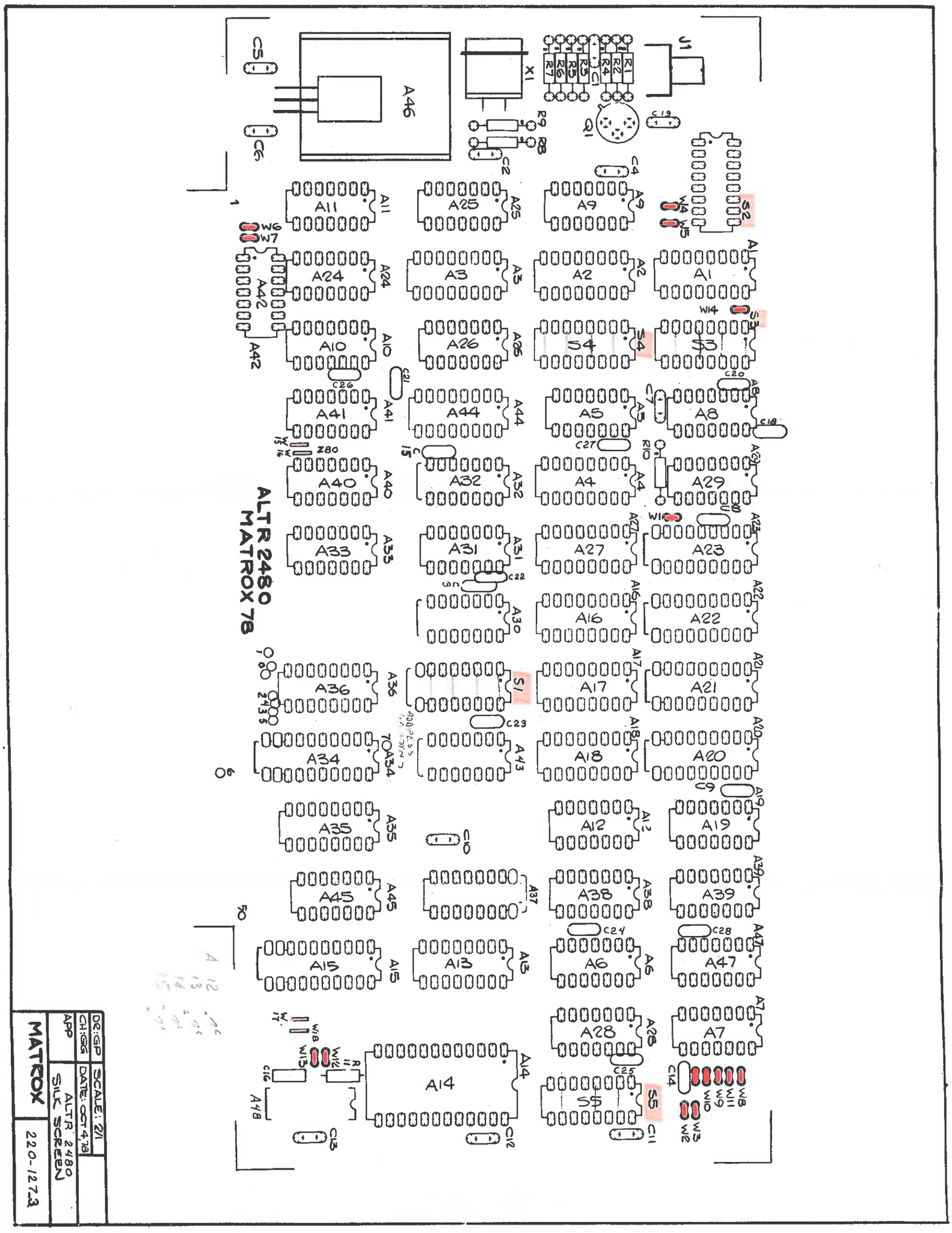
CODE	DESIGNATION	+5V	GND	MAKE FROM
74S163	A1, 2, 3	16	8	16
74LS390	A4	16	8	16
74LS393	A5	14	7	14
74LS74	A6, 7, 39, 42, 43	14	7	14
74LS21	A8, 41	14	7	14
74LS10	A9, 26, , 41	14	7	14
74LS11	A10	14	7	14
74LS02	A11, 29, , 47	14	7	14
74LS86	A12	14	7	14
74LS165	A13	16	8	16
2716	A14	24	12	24
74LS273	A15, 34	20	10	20
74LS157	A16, 17, 18	16	8	16
74LS00	A19, 38, 40,	14	7	14
2114	A20, 21, 22, 23	18	9	18
74LS32	A24	14	7	14
74LS04	A25	14	7	14
74LS368	A27	16	8	14
74LS08	A28, 32	14	7	14
74LS367	A30, 36, 37, 44	16	8	16
74LS25	A45	14	7	14
74LS14	A30			
74LS132	A33			

TYPE : ALTR-2480 /E5-
DATE : SEP 07 1990 6-I
SER. NO. : 1083
CUST. : A 1 0 0 S
STS : :

Matrox Electronic Systems Ltd.
MADE IN CANADA

MATROX ELECTRONIC SYSTEMS

Tst. Engr. 26/11/89	ALTR_2480.927.127-3	
Prod. Engr. 27/11/89		1 OF 1
QA 27/11/89		


ALTR 2480
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