MACROTECH

MSR-1

Technical Manual

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MSR SERIES TECHNICAL MANUAL

(Preliminary)

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INTRODUCTION

This manual provides information for installing and operating the MACROTECH MSR Series RAM boards in most of the currently popular S-100 systems.

This manual is organized in sections as follows:

CHAPTER 1 INTRODUCTION

Introduces and outlines the basics of the MSR Series product.

CHAPTER 2 INSTALLATION GUIDE

Contains configuration examples for specific environments organized onto individual pages for each application.

CHAPTER 3 CONFIGURATION SWITCH SETTINGS

Describes in detail the function of various switch settings, to aid in configuring for environments other than those described in Chapter 2.

CHAPTER 4 THEORY OF OPERATION

An explanation of the major functional circuits of the MSR. This chapter is best read while referring to the published logic diagrams at the rear of this manual.

APPENDICES

Additional information pertinent to configuration and operation of the MSR Series RAM boards.

1.1 PRODUCT DESCRIPTION

The Macrotech MSR is a high performance dynamic RAM designed to comply with IEEE-696 specifications and yet allow as much flexibility as possible in order to operate in a wide variety of S-100 computer environments.

Available in either a 256 or 512 kilobyte configuration, MSR Series RAM boards utilize 120 nanosecond access NMOS dynamic RAM chips.

The MSR's base-address may be set to begin on any 64 kilobyte boundary within the extended 16 megabyte S-100 address space.

The use of high-quality parts and MACROTECH's full one-year warranty assure long life and reliable service from this product.

INTRODUCTION

1.2 SYSTEM REQUIREMENTS

The MSR Series board is designed to occupy one position (slot) within a standard S-100 chassis. Physical dimensions of 5 inches by 10 inches wide with a nominal PC board thickness of .060 inches are called-out in the IEEE-696 specification.

Power requirement is 1.2 amps at the 8 volt supply line (pins 1 and 51 total) typical.

1.3 SPECIFICATIONS

Access Time - 123 nanoseconds typical, 166 guaranteed maximum. (performance guaranteed over full operating temperature range 0-70 deg. C).

Cycle Time - Less than 280 nanoseconds

Memory Devices - 64K X 1 dynamic NMOD RAMS, 120ns manufacturer's access specification.

Refresh - Full IEEE/696 refresh support (not bus-cycle dependent).On-board 15 microsecond timer with no cumulative error, exceeds RAM manufacturer's refresh timing requirements.

Parity - Byte parity generation and error detection. Jumper selectable. Software enable/disable via I/O port. LED indicator for parity error condition status.

Addressing - Board addressable on any 64K boundary within the S-100 IEEE/696 specified 16 Megabyte extended (24 bit) address range.

Data Transfer - Supports the IEEE/696 8/16 data transfer protocol.

Phantom - Phantom enable/disable jumper selectable. Cromemco and Alpha Micro special phantom schemes are supported.

PC Board - High quality 4-layer board with controlled dielectric. Fully solder-masked and silk-screened with component identification. Gold plated edge connector.

Power Consumption - 1.2 amps average (application dependent)
1.7 amps maximum (calculated worst-case) over full IEEE/696 supply voltage range, (+7.5 Volts to +11.5 Volts)

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CHAPTER 2 INSTALLATION GUIDE FOR SOME POPULAR CPU ENVIRONMENTS

This chapter contains configuration examples for specific environments organized onto individual pages for each application.

A pictorial diagram is presented for each example, showing graphically the locations of the jumper-switches and their settings as explained in the accompanying text.

The address switch settings have been omitted from the examples. A complete table of address switch settings are provided in Appendix A.

Due to the wide variety of S-100 environments, every possible configuration is not presented.

INSTALLATION GUIDE

2.1 LOMAS 8086

2.1.1 Description

The Lomas 8086 is a CPU board manufactured by Lomas Data Products of Westborough, MA. The Lomas 8086 CPU is based on the Intel 8086 16-bit microprocessor.

2.1.2 Operating Requirements

No special considerations are necessary when running in this environment.

2.1.3 Diagram

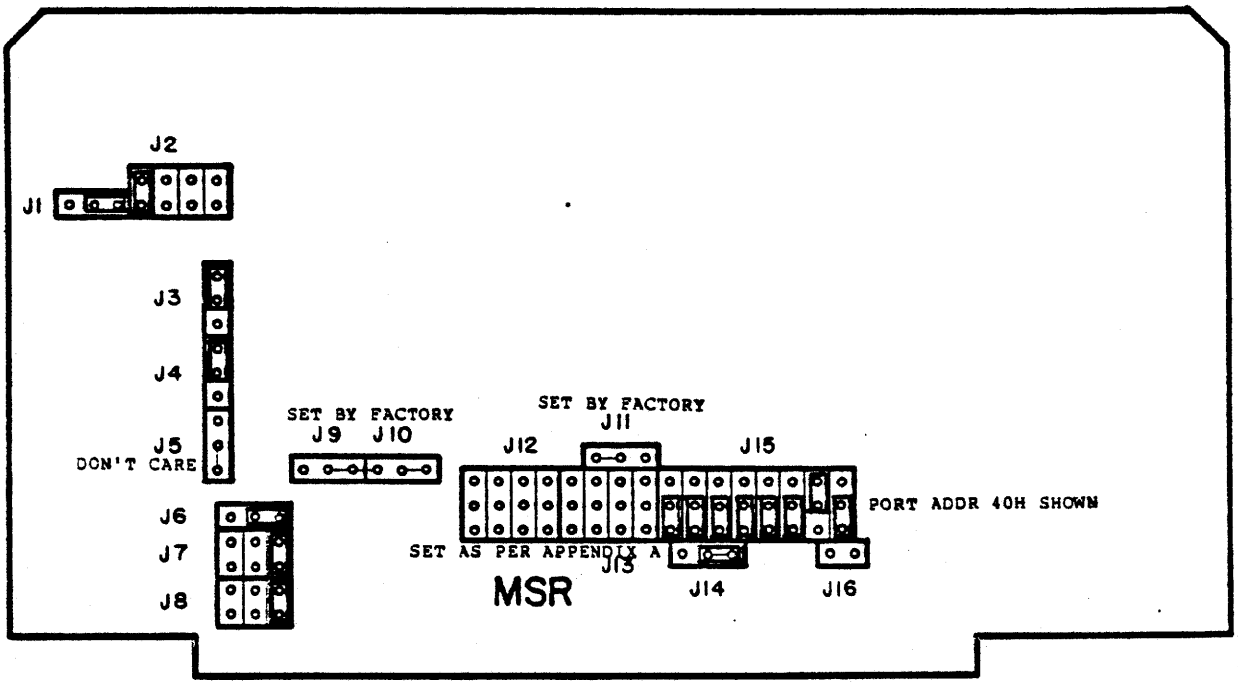

Figure 2-1
MSR Switch Settings for use with Lomas 8086

2.2 ALPHA-MICRO AM100/L

2.2.1 Description

The AM100/L is a CPU manufactured by Alpha-Micro Systems of Irvine California. The AM100/L processor, based on the Motorola 68000 microprocessor, deviates slightly from the IEEE-696 specification. The MSR is fully compatible with Alpha-Micro's version of the S-100 bus standard.

2.2.2 Operating Requirements

No special configuration or procedure is required to install the MSR in the ALPHA-MICRO AM100/L environment.

2.2.3 Diagram

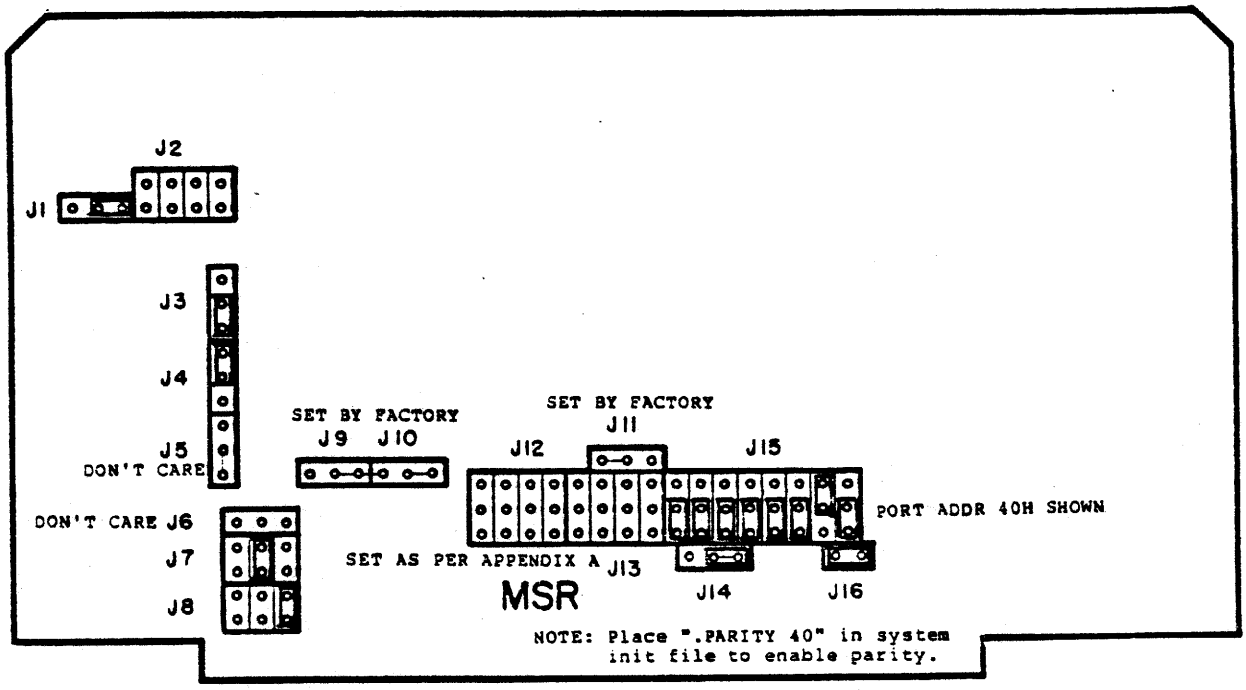

Figure 2-2
Switch Settings for use with AM100/L CPU

INSTALLATION GUIDE

2.2.4 Comments

The MSR Series exceeds access time requirements for the 8 MHz 68000 on the AM100/L. If you are using MSR as the only memory in the system, you can set the MR and MW jumpers on the AM100/L CPU board to zero. This disables all wait states selected on the AM100/L CPU.

Remember, if you use an AM720, AM710, MACROTECH MAX or other memories in the same chassis containing the MSR, the standard factory setting will have to be used. See Figure 2 below.

Factory	Standard Setting		MSR Only Environment	
	MR	MW	MR	MW
0	*=*	* *	*=*	*=*
1	* *	* *	* *	* *
2	* *	*=*	* *	* *
3	* *	* *	* *	* *
4	* *	* *	* *	* *

("=" indicates jumper installed)

2.3 ZENITH Z-100

2.3.1 Description

The Z-100 is a personal computer system manufactured by Zenith Data Systems. The Z-100 system is based on an 8085 and 8088 dual 8-bit microprocessor arrangement. The Z-100 normally comes shipped from the factory with either 128k or 192k of system memory on the mother board.

2.3.2 Operating Requirements

No special considerations or procedures are required to operate the MSR Series in the Z-100 environment.

2.3.3 Diagram

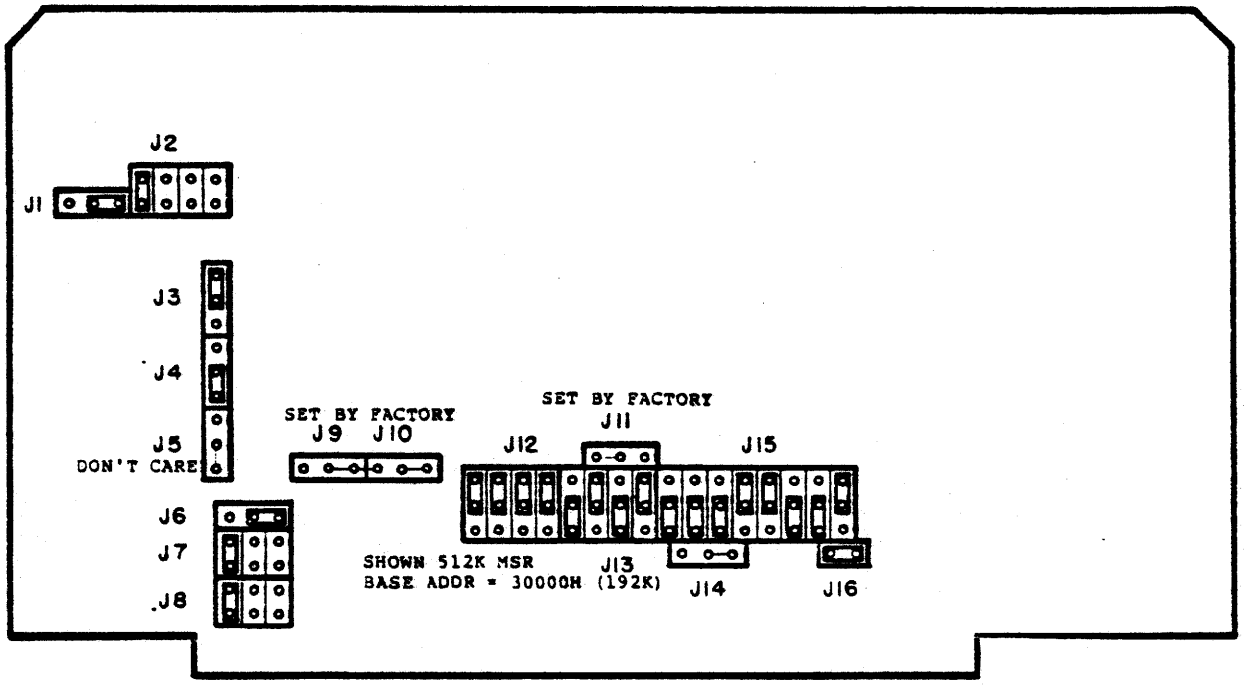

Figure 2-3
MSR Switch Settings for use with Z-100

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CONFIGURATION SWITCH SETTINGS

3.1 INTRODUCTION

This section is a quick summary of jumper options, primarily to assist you in setting up the MSR for environments not spelled-out in Chapter 2.

Most of the "switches" on the MSR board are groups of jumper posts. "Setting a switch" means shorting two of the posts in the switch together by slipping a shunt-jumper down onto them. (This kind of switch setup is more flexible, and far more reliable, than dip-switches. (Additionally, if a jumper should fail, it can be quickly and cheaply replaced without soldering.)

A few of the MSR's switches are bare pads with a "default jumper", a thin circuit trace, already in place between them. Ordinarily, these switches shouldn't have to be changed. If your system is one of the rare cases, simply cut the default trace and solder a jumper wire into the desired position.

CONFIGURATION SWITCH SETTINGS

3.2 CONFIGURATION SWITCH LOCATIONS

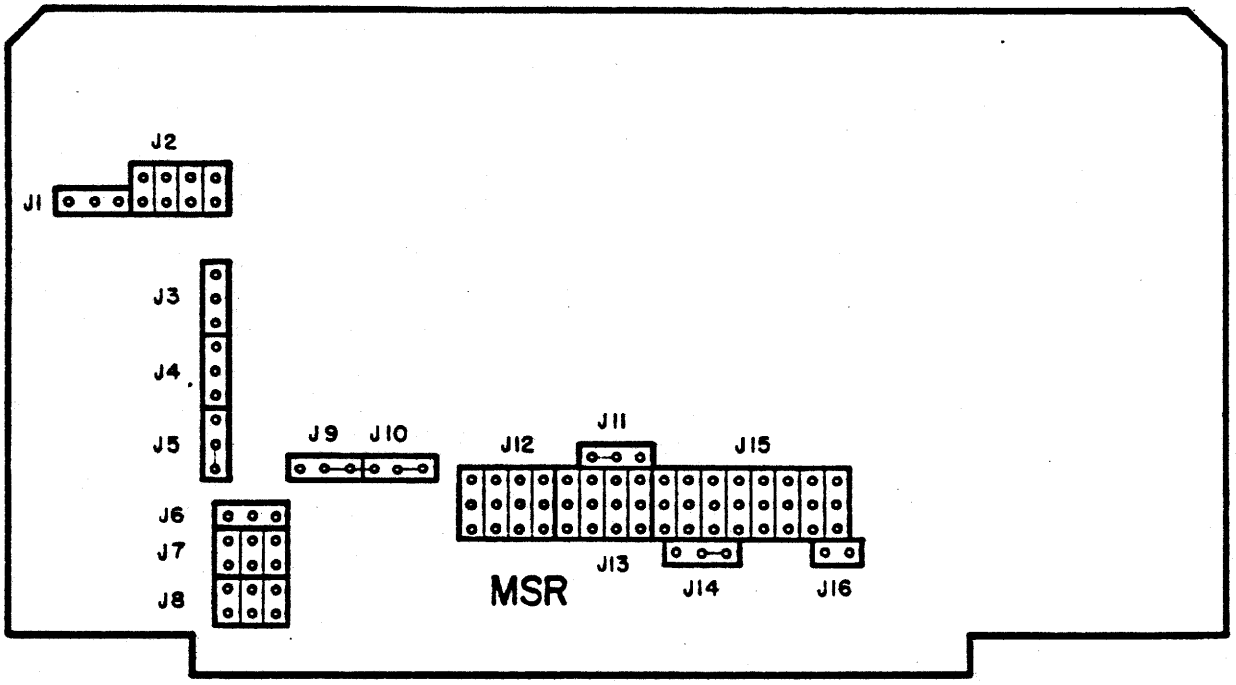


Figure 3-1
MSR Jumper Locations

3.3 MEMORY ADDRESS SELECTION

Jumper areas J12 and J13 control board "base-address" selection (the starting address for the contiguous block of memory occupied by the board). This base-address may be set to any 64k boundary.

Due to the logic which provides this extreme flexibility, the switch settings will vary for a given board base address depending upon the size of the memory array. For example, the address switch setting will be different for a 512k board addressed at zero than for a 256k board at the same address. The table in appendix A gives a complete table of switch settings.

3.4 SETTING BOARD SIZE

"Jumper-switch" J11 defines the memory population of the MSR RAM for the addressing logic. This switch should be set to the left (the default trace) for a 512k board. It is jumpered to the right for a 256k board. A 256k board will have only 36 RAM IC's installed.

3.5 CONTROL PORT ADDRESS

The MSR RAM utilizes one I/O port to control both parity operation and the Cromemco phantom scheme. The J15 switch area defines the this 8-bit I/O port address. Jumpers installed in the up position are considered a logical "1"; jumpers installed in the down position are considered a logical "0". These 8 switches are read RIGHT to LEFT in DESCENDING bit-significance (i.e. a desired port address of 0F1H would be set LEFT to RIGHT as 10001111).

3.6 CYCLE START OPTIONS

J7 allows several methods for starting memory cycles.

3.6.1 Alternate PSTVAL

This option is provided to allow the MSR RAM to function properly with environments that do not generate a properly timed PSTVAL.

The MSR Series RAM is able to generate its own cycle-start signal approximately 75 nanoseconds after the rising edge of PSYNC when this option is selected. Different timing may be configured by replacing C5 and/or R5 with components of different values. Most modern environments will not use this option.

3.6.2 Bus PSTVAL

Selecting this option allows the MSR RAM to start memory access cycles on the falling edge of PSTVAL (pin 25) while PSYNC (pin 76) is high on the S-100 bus. This is the most common method for cycle starts, and is standard for environments that adhere to the IEEE-696 bus standard.

3.6.3 Early Cycles

This option will start cycles on the rising edge of PSYNC. This option is advantageous for those environments that present address and status on the bus ahead of the PSYNC pulse.

All address and status signals must be valid at least 30 nano-seconds before PSYNC for this option to function properly. Select this option if you are putting the MSR into an Alpha Micro AM-100/L (68000 cpu) system.

CONFIGURATION SWITCH SETTINGS

3.6.4 Phi Cycle Start

This option combines the use of J7 and J6. Install a shunt-jumper vertically in the upper left hand corner of the J6/J7/J8 jumper area for this option (see Figure 3-1). Memory cycles will start when Phi (bus pin 24) goes low during the PSYNC strobe.

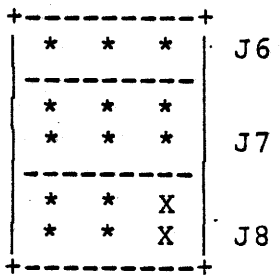
Installing a jumper in this position physically prevents a selecting J6 in a LEFT position. If you need J6 jumpered to the left, use proper wire and a wire-wrap tool to put it in.

3.7 PHANTOM CONTROL

J8 selects the desired phantom scheme. Three phantom schemes can be programmed into the J8 jumper area; a fourth scheme is available by doing a wire modification.

3.7.1 Phantom Disabled

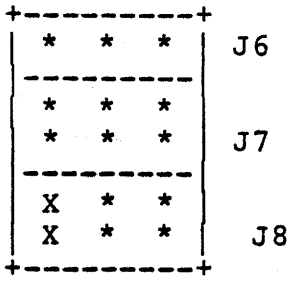
Selecting this option causes phantom to be ignored. The MSR memory will always be in a read/write (enabled) condition, regardless of the logic level on the bus phantom line, when J8 is installed to the right.



("X" indicates jumper installed)

3.7.2 Phantom Enabled

This option allows the MSR memory board to be disabled whenever pin 67 (PHANTOM*) is low. This is the most common use of phantom; it allows boot PROMs to be overlain by (addressed to the same location as) system memory.

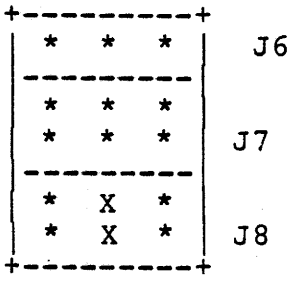


("X" indicates jumper installed)

3.7.3 Cromemco Phantom Scheme

This option disables the top 32k (8000 - ffff) of every 64k block of RAM until enabled by writing to the MSR memory control port.

This option should be used in Cromemco environments. The position of J5 becomes relevant when this option is selected. Normally, J5 should be set in the down position for the Cromemco environment.



("X" indicates jumper installed)

CONFIGURATION SWITCH SETTINGS

3.7.4 Shadow Phantom

Shadow phantom is a configuration where the MSR memory is in a write-only condition when phantom is active (bus pin 67 low). Enabling this feature requires a simple physical modification to the MSR.

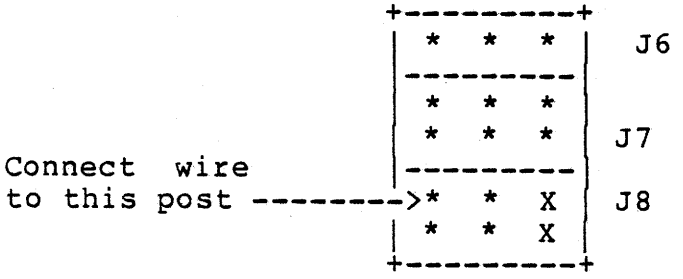
1. Cut pin 2 of the IC at location M12 (74F11) from the MSR PC board. Leave pin 2 long enough that a wire may be soldered to it.

2. Solder one end of a jumper wire to this cut IC leg.

3. Route the jumper wire to the J8 jumper area. The preferred method is to run the wire under the ICs on the component side of the board.

4. Wire wrap the other end of the jumper wire to the upper left hand pin in the J8 jumper area. See figure below:

5. Install a shunt-jumper in the rightmost position of the J8 jumper area as shown. This option is useful when the contents of the boot prom must be copied into RAM at start-up, or where the boot prom addressing logic asserts PHANTOM* for every memory access while it is enabled.



("X" indicates jumper installed)

3.8 PARITY ERROR ENABLE

J4 selects the method of enabling parity error.

When J4 is set in the up position, the parity error detection logic is enabled by the first write to the MSR I/O command port. It stays enabled until the system is reset.

When J4 is set in the down position, the error detection logic is both enabled and disabled via the sense of data bit 5 when the I/O command port is written.

When high (1), the error detection logic is enabled.

When low, the error detection logic is disabled.

Disabling the parity will de-assert the system's ERROR* line (S-100 pin 98) if an error had been previously detected. This ability can be used to implement an interrupt routine to report parity errors. See the section titled "Software Considerations" for some ideas on this subject.

3.9 ERROR STROBE CONTROL

The option switch J3 controls the duration of the parity error signal generated by the MSR RAM. If J3 is set in the up position, any indication of a parity error condition will be latched. If J3 is set in the down position, any error condition will be reported (by assertion of the ERROR* line) only until the end of the memory cycle in which the error occurs (ie: until the end of the PDBIN strobe).

3.10 BUS PARITY ERROR

Installation of the J16 jumper connects the parity error signal to pin 98 (ERROR*) of the S-100 bus. Removal of J16 will disconnect the parity error signal generated by the MSR from the bus. In the latter case, all other parity options discussed above will be "don't care" cases, since the S-100 signal ERROR* is the only way that the MSR Series RAM may report a parity error.

3.11 WAIT STATES

The MSR contains a highly flexible wait state configuration scheme. Jumpers J1, J2, J6, and J14 all affect wait state operation.

3.11.1 Number of Wait States

The J2 jumper area selects the desired number of wait states. Don't use more than one shunt-jumper in this area.

Putting the jumper in the leftmost position selects one wait state. Each position towards the right adds one more wait state, so that a jumper installed in the rightmost position selects four wait states.

The type of wait state(s) selected are determined by the position of J1.

CONFIGURATION SWITCH SETTINGS

3.11.2 Type of Waits

When J1 is set to the left, wait states will be inserted on every memory cycle, whether or not a refresh cycle is occurring.

When J1 is set to the right, it disables all wait states except when a memory request from the system and a refresh cycle occur at the same time.

The position of J2 (discussed above) will determine how many additional wait states are inserted in addition to the time required to complete the refresh and pending memory cycle.

3.11.3 Timing

J14 determines when wait states will be enabled. "Wait" states are asserted on the S-100 bus via pin 72 (READY) by pulling this signal line LOW (0 -or- "not READY").

Setting J14 to the right allows the wait state logic to place wait states on the bus when bus status and address have the MSR board selected. THIS IS THE STANDARD FACTORY SETTING, AND IT IS IMPLEMENTED VIA A CIRCUIT TRACE. This trace MUST BE CUT prior to attempting to install J14 to the left.

With J14 set left, the bus READY will not be affected until later in the cycle (i.e. after the "cycle start" discussed in section 3.6). This option was designed for use with CPUs that are able to honor WAITs asserted relatively late in the memory cycle.

The setting of J14 to the left also limits the number of wait states to one (1), effectively rendering the setting of J2 (see section 3.11.1) irrelevant.

Switch J6 allows clocking of the wait state counter on either the rising or falling edge of the bus clock (Phi) from pin 24.

Installation of J6 to the right synchronizes wait state timing to the falling edge of phi. This is the most common configuration.

Installation to the left will cause READY (bus pin 72) to change state on the rising edge of phi.

3.12 SUMMARY OF SWITCHES

3.12.1 Wait Enable

J1	Left	Memory wait states selected.
	Right	No memory wait states; additional wait states during arbitrated refresh cycles if J2 installed.

Note: J1 is a "don't care" if J2 is not installed.

3.12.2 Number of Waits Select

J2	Left	One clock count.
	Left center	Two clock counts.
	Right center	Three clock counts.
	Right	Four clock counts.

Caution: Install only one jumper in J2.

3.12.3 Error Strobe Control

J3	Up	Error strobe latched.
	Down	Error strobe pulsed.

3.12.4 Parity Enable

J4	Up	Enable upon any write to MSR I/O port.
	Down	Enable/disable via data bit 5, (0 = off; 1 = parity on).

3.12.5 CR Phantom Control Bit

J5	Up	Enable the disabled memory upon any write to MSR I/O port.
	Down	Enable the disabled memory only when data bit 0 is a "1".

J5 is a "don't care" unless J8 is in the center position.

3.12.6 Wait Clock Edge

J6	Left	Rising edge of Phi.
	Right	Falling edge of Phi.

J6 is a "don't care" if J2 is not installed.

CONFIGURATION SWITCH SETTINGS

3.12.7 Cycle Start

J7	Left	Bus PSTVAL.
	Center	Early cycle start.
	Right	Alternate PSTVAL.
	Left Upper	Phi cycle start. Combined use of J6 and J7.

3.12.8 Phantom Enable

J8	Left	Phantom enabled.
	Center	CR phantom (Cromemco).
	Right	Phantom disabled.

3.12.9 RAS Precharge

J9	Left	Delta 3
	Right	Delta 4

J9 is set by factory and should not be changed.

3.12.10 RAS Strobe

J10	Left	Delta 4
	Right	Delta 5

J10 is set by factory and should not be changed.

3.12.11 Board Size

J11	Left	512 kilobytes
	Right	256 kilobytes

3.12.12 Board Address

J12	4 ea. Up/Dn	See Appendix A for complete
J13	4 ea. Up/Dn	address table.

3.12.13 Ready Enable

J14	Left	Enabled via MRQ.
	Right	Enabled via SMEM.

3.12.14 I/O Port Address

J15	8 ea. Up/Dn	See Appendix B for complete table.

3.12.15 Error Strobe

J16	Installed	Connected to bus pin 98.
	Omitted	Disconnected.

This section describes in some detail the operation of the logic circuits comprising the MSR Series RAM board. Not intended as a complete discussion of each logical element, this chapter sets forth the basic theory of each major functional area and correlates these to the schematic diagram at the rear of this manual.

4.1 THEORY OF OPERATION

An attempt will be made to discuss each logical area of the board in approximate chronological sequence as events on the bus cause the transfer of data to or from the appropriate RAM storage cells.

4.1.1 BUS INTERFACE

The full 24-bit "extended" S-100 address is divided into two sections.

(a) The least-signifigant 16 bits feed directly from the bus into two 8-bit buffers (74F244) at IC locations K7 and M7. The lower 8 (A0 through A7) are then immediately presented to an address comparator (at location H7) for decoding of the I/O port address in the case of I/O operations.

The outputs of the address buffers become Buffered Address terms (BA0, BA1, BA2, etc.)

(b) The upper 8 address lines (A16 through A23) are used to determine the "base address" match through the two ADDER ICs (74F283) at locations K8 and M8.

An exception to this strict division is A16, which is presented to both sections (a) and (b) above.

STATUS signals are buffered at various gates and inverters near to the point of their use. Care has been taken not to exceed one TTL load on any single STATUS line from the bus.

THEORY OF OPERATION

CONTROL lines (pWR*, pSYNC, pSTVAL*, etc.) are also buffered at many different places and ICs on the board. In a manner similar to the treatment of bus loading for the STATUS signals, care has been taken not to exceed one TTL load on any single line from the bus.

The bus signals SIXTN*, RDY and ERROR* are driven by the MSR Series board via the open-collector device (74F38) at location K6.

4.1.2 I/O OPERATIONS

The Parity Error and Phantom control port has been provided with the capability of accepting Port Output instructions (no Input data is available).

The standard 8-bit port addressing (1 of 256) is decoded through the address comparator at location H7. If the STATUS signal SOUT is true and the lower 8 address lines compare with the switch settings in the J15 field, the signal OUTSEL* is generated which will affect two signals;

(a) pWRB* will be allowed to pass through one AND gate of the 74F08 at location E2 to strobe the data bits D0 and/or D5 into the flip-flops (74F113) at locations E1 and G2 for the purposes of disabling the Parity Error Detect logic or the Cromemco Phantom scheme respectively.

(b) The enable logic for the data buffer (74F244) at location K9 will be forced true so that bus data is allowed to reach the inputs of the JK flip-flops mentioned in (a) above.

4.1.3 THE CYCLE

One complete access of the MSR series board is comprised of four distinct operations or phases;

The detection of appropriate S100 ADDRESS signals to indicate attempted access to an individual address location contained within this MSR RAM board.

The decoding of STATUS signals indicating a proper MEMORY (or in the case of the single MSR control port, I/O) read or write operation is in progress.

The routing of CONTROL signals for purposes of synchronizing the transfer of data between the RAM array and the system bus.

TERMINATION of the cycle in a well-defined manner allows a set-up period for subsequent cycles; or it allows other types of cycle (e.g. REFRESH) to begin.

4.1.3.1 ADDRESSING THE MSR

Addresses for I/O operations are described in paragraph 4.1.1-(a) above.

Addresses for MEMORY cycles are handled as follows:

Buffered Address terms BA1 through BA16 are presented directly to the address inputs of the VLSI RAM Controller IC (AM2964B) located at D8 which multiplexes these 16 signals out to the RAM array, 8 at a time, during the appropriate Row or Column Address Strobe (RAS or CAS).

Address bits A16 through A23, brought to the 74F283's at M5 and K5, are ADDed to the jumper-switch settings from the fields J12 and J13.

IF

the outputs of the ADDer IC at location M5 are ALL HIGH

AND

the most signifigant bit(s) of the ADDer IC at location K5 is HIGH (upper 2 bits if configured for 256 kilobytes)

AND

PHANTOM* is either de-selected or FALSE

THEN

A true ADDRESS SELECT term is generated at pin 10 of the 74F02 at location K4.

Two outputs from the ADDer IC at location K5 are used as ROW SELECT lines (RSEL0 and RSEL1). These signals go directly to the VLSI DYNAMIC RAM CONTROLLER IC at location D8 in order that this device will select the proper ROWs of RAM ICs.

4.1.3.2 BUS STATUS SIGNALS TO THE MSR

The generation of the ADDRESS SELECT term from pin 10 of the 74F02 at location K4 will allow the active STATUS signal SWO* or SMEMR to be gated to one of the D inputs of the 74F74 at location H2.

These STATUS signals, after being gated through the 74F11 at M12, will be ORed to form an enable term for the SIXTN* (sixteen bit transfer acknowledge) where it is gated onto the S-100 bus from pin 6 of the 74F38 at K6.

4.1.3.3 CONTROL SIGNALS

Now that the ADDRESS and the STATUS have been resolved, and the SXTRQ* has been satisfied with the SIXTN* output if appropriate, the control signals pSYNC and pSTVAL* will actually synchronize the beginning of the RAM access.

The STATUS identifying a memory Read or Write operation was gated to the D inputs of the 74F74 at H2 in paragraph 4.1.3.2 above. The clock to latch this status is necessary to actually begin the access and this clock may be derived in one of several ways:

pSTVAL* from the S-100 bus, if jumpered to pin 2 of the 74F02 at location K4, will generate the signal CYCSTB (CYCleSTroBe) at pin 1 of this IC, which in turn clocks the flip-flop at location H2 (both halves).

The ALTERNATE pSTVAL* will create nominal cycle-start timing in environments that do not generate a properly timed pSTVAL*. This is accomplished through:

(a) An inverted pSYNC is deliberately delayed approximately 25 nano-seconds through the RC network R4/C4 and one gate of the 74F32 at L2.

(b) If pin 2 of the 74F02 at K4 is jumpered to GROUND via J7, then this delayed-inverted pSYNC at pin 3 of the same gate will generate CYCSTB approximately 4 nanoseconds later.

(c) If pin 2 of the 74F02 at K4 is jumpered to the double-inverted PHI (pin 24 clock) from pin 10 of the inverter IC at M3, then after the arrival at pin 3 of the same gate of the delayed-inverted pSYNC, CYCSTB will occur approximately 4 nanoseconds after the low-going edge of PHI.

(d) If pin 2 of the 74F02 at K4 is jumpered to the inverted PHI (pin 24 clock) from pin 10 of the inverter IC at M3, then after the arrival at pin 3 of the same gate of the delayed-inverted pSYNC, CYCSTB will occur approximately 4 nanoseconds after the rising edge of PHI.

CYCSTB latches through the condition of the S-100 STATUS signals SWO* and SMEMR at the time these signals were guaranteed valid, and the latch output terms WR or RD identifies which type of memory operation is in progress throughout the remainder of the current cycle.

WR and RD are ORed in one gate of the 74F32 at location H3 so that either one of them being active during a cycle causes MRQ (Memory ReQuest) and MRQ* to be TRUE also.

The only function of MRQ is to enable WAITS (S-100 RDY FALSE) onto the bus during accesses to THIS BOARD only if J14 is set to the left.

The function of MRQ* is to inhibit the beginning of a REFRESH cycle during any portion of a MEMORY ACCESS cycle, (see the section on REFRESH CYCLES), and to tell the RAM CONTROLLER IC (via pin 36 of the AM2964B) that a request is pending.

RD and WR are input to the 74F64 at K3 where they are qualified by:

A completed RAS precharge time from the previous cycle as determined by the 74F32 section jumpered to pins 6, 8, and 10 of the DELAY LINE.

No REFRESH in progress as determined by the Q* output from pin 6 of the 74F74 at K1.

In the case of WR only, the additional qualification of an active pWR* strobe at the S-100 bus.

The output of this 74F64 is the term RASI*. The term RASI* going true (low) starts the pulse through the DELAY LINE where it generates the main timing required by the NMOS DYNAMIC RAM ICs, including CASI* as output from pin 8 of the 74F32 at H3.

RASI* and CASI* are presented to the VLSI RAM CONTROLLER IC where they synchronize the Controller IC's output signals to the RAMs.

pDBIN is used as a term of the signal enabling the 74F373 tri-state latches at H10, K10, and H9 onto the S-100 bus at the correct time. It is gated with the term RDSEL which was generated in one half of the latch at location F1 when CYCSTB was TRUE and RD went TRUE, clearing the latch. The TRAILING EDGE (low-going) of an inverted pDBIN becomes the clock for this latch, effectively SETTING it at the end of the READ STROBE (pDBIN) causing RDSEL to go false again.

The term RDSEL is used to qualify (gate) any PARITY ERROR signals from either the EVEN or ODD Parity Detect ICs at K11 or H11. Therefore, pDBIN is responsible for the TIMING of the Parity

Error signal allowed to be presented to the PARITY ERROR LATCH at location G2.

4.1.3.4 TERMINATING THE CYCLE

When the term RASI* went true (low) in the discussion above, it also was inverted in one section of the inverter IC at location M3. This output from pin 8 of the inverter IC performed several functions:

It was fed around to pin 3 of the RASI* generator IC (74F64) at location K3, thus becoming a term of itself and latching RASI* true for a minimum RASI* time equal to delta 4 or delta 5 in duration, depending on the jumper settings of J9 and J10. This latching effect will guarantee minimum RASI* width in the case of a short-lived triggering event such as the pulse generated by the output of pin 13 of the 74F02 at location K4 when a REFRESH cycle is started.

This signal also allowed the WAIT STATE latch (location K2) clock to occur on the trailing edge of pSYNCB* at the 74F10 pin 12 at location G1.

The leading (rising) edge of this signal CLOCKED pin 11 of the 74F74 at K2, latching its outputs in the state identifying this cycle as a MEMORY CYCLE and not a REFRESH CYCLE.

Now the conditions are set for ending the cycle in the following manner:

The delta 4 or delta 5 time-out occurs as described above, and the low-going signal from pin 11 of the 74F32 at H3 removes the qualifiers to all four sections of the input gates in the RASI* generator IC.

The inverted RASI* returns to a LOW as RASI* goes FALSE (high).

This signal goes to pin 4 of the AND gate at H3 (74F32) and since MSEL* is stll low until the delay line has a chance to propagate the now-high RASI* to delta 1, H3 pin 6 presents a low output.

Since a MEMORY CYCLE had been previously latched in the half of the flip-flop at K2 holding the cycle identification, one section of the 74F32 at L2 will now present a LOW on the output at pin 11.

This LOW signal will; (1) Reset both halves of the 74F74 at H2, resetting both RD and WR. (2) Reset the WAIT STATE latch at location K2.

4.1.4 REFRESH CYCLES

A 7555 TIMER IC at location D1 is set to run with a period near 15 microseconds. The rising edge of its output will clock a flip-flop in one-half of the IC at M2 and the subsequent stages in K1 and the other half of M2 ensure that the refresh cycle is synchronized to the S-100 bus.

The output of the last stage of the synchronizer on pin 5 of the 74F74 at M2, is fed to a gate of the 74F10 at location G1. If pSYNC is presently FALSE and MRQ* (discussed in section 4.1.3.3) also indicates that no memory cycle is in process, then the flip-flop in one half of the IC at K1 is forced SET (via the preset input) forcing its output term REF* true (low).

The low-going signal REF* will cause a pulse into the 74F64 RASI* generating IC at K3, via the pulse-making network of R6, C6, and one gate of the 74F02 at location K4.

This pulse will self-latch as described in section 4.1.3.4, and generate the required RASI* for the REFRESH cycle.

The now low REF* signal also resets the three flip-flops in the synchronizer circuit and force-presets the WAIT STATE latch at K2 so that should the board be addressed and the S-100 status signals indicate a MEMORY type of operation, pin 72 on the S-100 bus (RDY) would be immediately pulled false (low), causing a WAIT condition on the bus.

The last task of the REF* signal is to tell the AM2964B via pin 25 that the current RASI* signal is associated with a REFRESH cycle, so that the RAM CONTROLLER IC will properly issue signals to the NMOS DYNAMIC RAM ICs for a REFRESH operation.

THEORY OF OPERATION

J1 Right
2 ~~Ø~~ 3rd from left Jumpered
~~3 Ø~~
~~4 Jumper~~
~~5 Ø~~

J3 up
J4 up

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J6 Right
J7 Left
J8 Left

BASE ADDRESS SWITCH TABLES

Memory Size/Address				Jumper Setting	
256K		512K		J12	J13
FD0000	16,192K	F90000	15,936K	Up Up Up Up	Up Up Up Up
FE0000	16,256K	FA0000	16,000K	Up Up Up Up	Up Up Up Dn
FF0000	16,320K	FB0000	16,064K	Up Up Up Up	Up Up Dn Up
000000	0K	FC0000	16,128K	Up Up Up Up	Up Up Dn Dn
010000	64K	FD0000	16,192K	Up Up Up Up	Up Dn Up Up
020000	128K	FE0000	16,256K	Up Up Up Up	Up Dn Up Dn
030000	192K	FF0000	16,320K	Up Up Up Up	Up Dn Dn Up
040000	256K	000000	0K	Up Up Up Up	Up Dn Dn Dn
050000	320K	010000	64K	Up Up Up Up	Dn Up Up Up
060000	384K	020000	128K	Up Up Up Up	Dn Up Up Dn
070000	448K	030000	192K	Up Up Up Up	Dn Up Dn Up
080000	512K	040000	256K	Up Up Up Up	Dn Up Dn Dn
090000	576K	050000	320K	Up Up Up Up	Dn Dn Up Up
0A0000	640K	060000	384K	Up Up Up Up	Dn Dn Up Dn
0B0000	704K	070000	448K	Up Up Up Up	Dn Dn Dn Up
0C0000	768K	080000	512K	Up Up Up Up	Dn Dn Dn Dn
0D0000	832K	090000	576K	Up Up Up Dn	Up Up Up Up
0E0000	896K	0A0000	640K	Up Up Up Dn	Up Up Up Dn
0F0000	960K	0B0000	704K	Up Up Up Dn	Up Up Dn Up
100000	1,024K	0C0000	768K	Up Up Up Dn	Up Up Dn Dn
110000	1,088K	0D0000	832K	Up Up Up Dn	Up Dn Up Up
120000	1,152K	0E0000	896K	Up Up Up Dn	Up Dn Up Dn
130000	1,216K	0F0000	960K	Up Up Up Dn	Up Dn Dn Up
140000	1,280K	100000	1,024K	Up Up Up Dn	Up Dn Dn Dn
150000	1,344K	110000	1,088K	Up Up Up Dn	Dn Up Up Up
160000	1,408K	120000	1,152K	Up Up Up Dn	Dn Up Up Dn
170000	1,472K	130000	1,216K	Up Up Up Dn	Dn Up Dn Up
180000	1,536K	140000	1,280K	Up Up Up Dn	Dn Up Dn Dn
190000	1,600K	150000	1,344K	Up Up Up Dn	Dn Dn Up Up
1A0000	1,664K	160000	1,408K	Up Up Up Dn	Dn Dn Up Dn
1B0000	1,728K	170000	1,472K	Up Up Up Dn	Dn Dn Dn Up
1C0000	1,792K	180000	1,536K	Up Up Up Dn	Dn Dn Dn Dn
1D0000	1,856K	190000	1,600K	Up Up Dn Up	Up Up Up Up
1E0000	1,920K	1A0000	1,664K	Up Up Dn Up	Up Up Up Dn
1F0000	1,984K	1B0000	1,728K	Up Up Dn Up	Up Up Dn Up
200000	2,048K	1C0000	1,792K	Up Up Dn Up	Up Up Dn Dn
210000	2,112K	1D0000	1,856K	Up Up Dn Up	Up Dn Up Up
220000	2,176K	1E0000	1,920K	Up Up Dn Up	Up Dn Up Dn
230000	2,240K	1F0000	1,984K	Up Up Dn Up	Up Dn Dn Up
240000	2,304K	200000	2,048K	Up Up Dn Up	Up Dn Dn Dn
250000	2,368K	210000	2,112K	Up Up Dn Up	Dn Up Up Up
260000	2,432K	220000	2,176K	Up Up Dn Up	Dn Up Up Dn
270000	2,496K	230000	2,240K	Up Up Dn Up	Dn Up Dn Up
280000	2,560K	240000	2,304K	Up Up Dn Up	Dn Up Dn Dn
290000	2,624K	250000	2,368K	Up Up Dn Up	Dn Dn Up Up
2A0000	2,688K	260000	2,432K	Up Up Dn Up	Dn Dn Up Dn
2B0000	2,752K	270000	2,496K	Up Up Dn Up	Dn Dn Dn Up

BASE ADDRESS SWITCH TABLES

Memory Size/Address				Jumper Setting	
256K		512K		J12	J13
2C0000	2,816K	280000	2,560K	Up Up Dn Up	Dn Dn Dn Dn
2D0000	2,880K	290000	2,624K	Up Up Dn Dn	Up Up Up Up
2E0000	2,944K	2A0000	2,688K	Up Up Dn Dn	Up Up Up Dn
2F0000	3,008K	2B0000	2,752K	Up Up Dn Dn	Up Up Dn Up
300000	3,072K	2C0000	2,816K	Up Up Dn Dn	Up Up Dn Dn
310000	3,136K	2D0000	2,880K	Up Up Dn Dn	Up Dn Up Up
320000	3,200K	2E0000	2,944K	Up Up Dn Dn	Up Dn Up Dn
330000	3,264K	2F0000	3,008K	Up Up Dn Dn	Up Dn Dn Up
340000	3,328K	300000	3,072K	Up Up Dn Dn	Up Dn Dn Dn
350000	3,392K	310000	3,136K	Up Up Dn Dn	Dn Up Up Up
360000	3,456K	320000	3,200K	Up Up Dn Dn	Dn Up Up Dn
370000	3,520K	330000	3,264K	Up Up Dn Dn	Dn Up Dn Up
380000	3,584K	340000	3,328K	Up Up Dn Dn	Dn Up Dn Dn
390000	3,648K	350000	3,392K	Up Up Dn Dn	Dn Dn Up Up
3A0000	3,712K	360000	3,456K	Up Up Dn Dn	Dn Dn Up Dn
3B0000	3,776K	370000	3,520K	Up Up Dn Dn	Dn Dn Dn Up
3C0000	3,840K	380000	3,584K	Up Up Dn Dn	Dn Dn Dn Dn
3D0000	3,904K	390000	3,648K	Up Dn Up Up	Up Up Up Up
3E0000	3,968K	3A0000	3,712K	Up Dn Up Up	Up Up Up Dn
3F0000	4,032K	3B0000	3,776K	Up Dn Up Up	Up Up Dn Up
400000	4,096K	3C0000	3,840K	Up Dn Up Up	Up Up Dn Dn
410000	4,160K	3D0000	3,904K	Up Dn Up Up	Up Dn Up Up
420000	4,224K	3E0000	3,968K	Up Dn Up Up	Up Dn Up Dn
430000	4,288K	3F0000	4,032K	Up Dn Up Up	Up Dn Dn Up
440000	4,352K	400000	4,096K	Up Dn Up Up	Up Dn Dn Dn
450000	4,416K	410000	4,160K	Up Dn Up Up	Dn Up Up Up
460000	4,480K	420000	4,224K	Up Dn Up Up	Dn Up Up Dn
470000	4,544K	430000	4,288K	Up Dn Up Up	Dn Up Dn Up
480000	4,608K	440000	4,352K	Up Dn Up Up	Dn Up Dn Dn
490000	4,672K	450000	4,416K	Up Dn Up Up	Dn Dn Up Up
4A0000	4,736K	460000	4,480K	Up Dn Up Up	Dn Dn Up Dn
4B0000	4,800K	470000	4,544K	Up Dn Up Up	Dn Dn Dn Up
4C0000	4,864K	480000	4,608K	Up Dn Up Up	Dn Dn Dn Dn
4D0000	4,928K	490000	4,672K	Up Dn Up Dn	Up Up Up Up
4E0000	4,992K	4A0000	4,736K	Up Dn Up Dn	Up Up Up Dn
4F0000	5,056K	4B0000	4,800K	Up Dn Up Dn	Up Up Dn Up
500000	5,120K	4C0000	4,864K	Up Dn Up Dn	Up Up Dn Dn
510000	5,184K	4D0000	4,928K	Up Dn Up Dn	Up Dn Up Up
520000	5,248K	4E0000	4,992K	Up Dn Up Dn	Up Dn Up Dn
530000	5,312K	4F0000	5,056K	Up Dn Up Dn	Up Dn Dn Up
540000	5,376K	500000	5,120K	Up Dn Up Dn	Up Dn Dn Dn
550000	5,440K	510000	5,184K	Up Dn Up Dn	Dn Up Up Up
560000	5,504K	520000	5,248K	Up Dn Up Dn	Dn Up Up Dn
570000	5,568K	530000	5,312K	Up Dn Up Dn	Dn Up Dn Up
580000	5,632K	540000	5,376K	Up Dn Up Dn	Dn Up Dn Dn
590000	5,696K	550000	5,440K	Up Dn Up Dn	Dn Dn Up Up
5A0000	5,760K	560000	5,504K	Up Dn Up Dn	Dn Dn Up Dn

BASE ADDRESS SWITCH TABLES

Memory Size/Address				Jumper Setting							
256K		512K		J12				J13			
5B0000	5,824K	570000	5,568K	Up	Dn	Up	Dn	Dn	Dn	Dn	Up
5C0000	5,888K	580000	5,632K	Up	Dn	Up	Dn	Dn	Dn	Dn	Dn
5D0000	5,952K	590000	5,696K	Up	Dn	Dn	Up	Up	Up	Up	Up
5E0000	6,016K	5A0000	5,760K	Up	Dn	Dn	Up	Up	Up	Up	Dn
5F0000	6,080K	5B0000	5,824K	Up	Dn	Dn	Up	Up	Up	Dn	Up
600000	6,144K	5C0000	5,888K	Up	Dn	Dn	Up	Up	Up	Dn	Dn
610000	6,208K	5D0000	5,952K	Up	Dn	Dn	Up	Up	Dn	Up	Up
620000	6,272K	5E0000	6,016K	Up	Dn	Dn	Up	Up	Dn	Up	Dn
630000	6,336K	5F0000	6,080K	Up	Dn	Dn	Up	Up	Dn	Dn	Up
640000	6,400K	600000	6,144K	Up	Dn	Dn	Up	Up	Dn	Dn	Dn
650000	6,464K	610000	6,208K	Up	Dn	Dn	Up	Dn	Up	Up	Up
660000	6,528K	620000	6,272K	Up	Dn	Dn	Up	Dn	Up	Up	Dn
670000	6,592K	630000	6,336K	Up	Dn	Dn	Up	Dn	Up	Dn	Up
680000	6,656K	640000	6,400K	Up	Dn	Dn	Up	Dn	Up	Dn	Dn
690000	6,720K	650000	6,464K	Up	Dn	Dn	Up	Dn	Dn	Up	Up
6A0000	6,784K	660000	6,528K	Up	Dn	Dn	Up	Dn	Dn	Up	Dn
6B0000	6,848K	670000	6,592K	Up	Dn	Dn	Up	Dn	Dn	Dn	Up
6C0000	6,912K	680000	6,656K	Up	Dn	Dn	Up	Dn	Dn	Dn	Dn
6D0000	6,976K	690000	6,720K	Up	Dn	Dn	Dn	Up	Up	Up	Up
6E0000	7,040K	6A0000	6,784K	Up	Dn	Dn	Dn	Up	Up	Up	Dn
6F0000	7,104K	6B0000	6,848K	Up	Dn	Dn	Dn	Up	Up	Dn	Up
700000	7,168K	6C0000	6,912K	Up	Dn	Dn	Dn	Up	Up	Dn	Dn
710000	7,232K	6D0000	6,976K	Up	Dn	Dn	Dn	Up	Dn	Up	Up
720000	7,296K	6E0000	7,040K	Up	Dn	Dn	Dn	Up	Dn	Up	Dn
730000	7,360K	6F0000	7,104K	Up	Dn	Dn	Dn	Up	Dn	Dn	Up
740000	7,424K	700000	7,168K	Up	Dn	Dn	Dn	Up	Dn	Dn	Dn
750000	7,488K	710000	7,232K	Up	Dn	Dn	Dn	Dn	Up	Up	Up
760000	7,552K	720000	7,296K	Up	Dn	Dn	Dn	Dn	Up	Up	Dn
770000	7,616K	730000	7,360K	Up	Dn	Dn	Dn	Dn	Up	Dn	Up
780000	7,680K	740000	7,424K	Up	Dn	Dn	Dn	Dn	Up	Dn	Dn
790000	7,744K	750000	7,488K	Up	Dn	Dn	Dn	Dn	Dn	Up	Up
7A0000	7,808K	760000	7,552K	Up	Dn	Dn	Dn	Dn	Dn	Up	Dn
7B0000	7,872K	770000	7,616K	Up	Dn	Dn	Dn	Dn	Dn	Dn	Up
7C0000	7,936K	780000	7,680K	Up	Dn	Dn	Dn	Dn	Dn	Dn	Dn
7D0000	8,000K	790000	7,744K	Dn	Up	Up	Up	Up	Up	Up	Up
7E0000	8,064K	7A0000	7,808K	Dn	Up	Up	Up	Up	Up	Up	Dn
7F0000	8,128K	7B0000	7,872K	Dn	Up	Up	Up	Up	Up	Dn	Up
800000	8,192K	7C0000	7,936K	Dn	Up	Up	Up	Up	Up	Dn	Dn
810000	8,256K	7D0000	8,000K	Dn	Up	Up	Up	Up	Dn	Up	Up
820000	8,320K	7E0000	8,064K	Dn	Up	Up	Up	Up	Dn	Up	Dn
830000	8,384K	7F0000	8,128K	Dn	Up	Up	Up	Up	Dn	Dn	Up
840000	8,448K	800000	8,192K	Dn	Up	Up	Up	Up	Dn	Dn	Dn
850000	8,512K	810000	8,256K	Dn	Up	Up	Up	Dn	Up	Up	Up
860000	8,576K	820000	8,320K	Dn	Up	Up	Up	Dn	Up	Up	Dn
870000	8,640K	830000	8,384K	Dn	Up	Up	Up	Dn	Up	Dn	Up
880000	8,704K	840000	8,448K	Dn	Up	Up	Up	Dn	Up	Dn	Dn
890000	8,768K	850000	8,512K	Dn	Up	Up	Up	Dn	Dn	Up	Up

BASE ADDRESS SWITCH TABLES

Memory Size/Address				Jumper Setting							
256K		512K		J12				J13			
8A0000	8,832K	860000	8,576K	DN	Up	Up	Up	Dn	Dn	Up	Dn
8B0000	8,896K	870000	8,640K	Dn	Up	Up	Up	Dn	Dn	Dn	Up
8C0000	8,960K	880000	8,704K	Dn	Up	Up	Up	Dn	Dn	Dn	Dn
8D0000	9,024K	890000	8,768K	Dn	Up	Up	Dn	Up	Up	Up	Up
8E0000	9,088K	8A0000	8,832K	Dn	Up	Up	Dn	Up	Up	Up	Dn
8F0000	9,152K	8B0000	8,896K	Dn	Up	Up	Dn	Up	Up	Dn	Up
900000	9,216K	8C0000	8,960K	Dn	Up	Up	Dn	Up	Up	Dn	Dn
910000	9,280K	8D0000	9,024K	Dn	Up	Up	Dn	Up	Dn	Up	Up
920000	9,344K	8E0000	9,088K	Dn	Up	Up	Dn	Up	Dn	Up	Dn
930000	9,408K	8F0000	9,152K	Dn	Up	Up	Dn	Up	Dn	Dn	Up
940000	9,472K	900000	9,216K	Dn	Up	Up	Dn	Up	Dn	Dn	Dn
950000	9,536K	910000	9,280K	Dn	Up	Up	Dn	Dn	Up	Up	Up
960000	9,600K	920000	9,344K	Dn	Up	Up	Dn	Dn	Up	Up	Dn
970000	9,664K	930000	9,408K	Dn	Up	Up	Dn	Dn	Up	Dn	Up
980000	9,728K	940000	9,472K	Dn	Up	Up	Dn	Dn	Up	Dn	Dn
990000	9,792K	950000	9,536K	Dn	Up	Up	Dn	Dn	Dn	Up	Up
9A0000	9,856K	960000	9,600K	Dn	Up	Up	Dn	Dn	Dn	Up	Dn
9B0000	9,920K	970000	9,664K	Dn	Up	Up	Dn	Dn	Dn	Dn	Up
9C0000	9,984K	980000	9,728K	Dn	Up	Up	Dn	Dn	Dn	Dn	Dn
9D0000	10,048K	990000	9,792K	Dn	Up	Dn	Up	Up	Up	Up	Up
9E0000	10,112K	9A0000	9,856K	Dn	Up	Dn	Up	Up	Up	Up	Dn
9F0000	10,176K	9B0000	9,920K	Dn	Up	Dn	Up	Up	Up	Dn	Up
A00000	10,240K	9C0000	9,984K	Dn	Up	Dn	Up	Up	Up	Dn	Dn
A10000	10,304K	9D0000	10,048K	Dn	Up	Dn	Up	Up	Dn	Up	Up
A20000	10,368K	9E0000	10,112K	Dn	Up	Dn	Up	Up	Dn	Up	Dn
A30000	10,432K	9F0000	10,176K	Dn	Up	Dn	Up	Up	Dn	Dn	Up
A40000	10,496K	A00000	10,240K	Dn	Up	Dn	Up	Up	Dn	Dn	Dn
A50000	10,560K	A10000	10,304K	Dn	Up	Dn	Up	Dn	Up	Up	Up
A60000	10,624K	A20000	10,368K	Dn	Up	Dn	Up	Dn	Up	Up	Dn
A70000	10,688K	A30000	10,432K	Dn	Up	Dn	Up	Dn	Up	Dn	Up
A80000	10,752K	A40000	10,496K	Dn	Up	Dn	Up	Dn	Up	Dn	Dn
A90000	10,816K	A50000	10,560K	Dn	Up	Dn	Up	Dn	Dn	Up	Up
AA0000	10,880K	A60000	10,624K	Dn	Up	Dn	Up	Dn	Dn	Up	Dn
AB0000	10,944K	A70000	10,688K	Dn	Up	Dn	Up	Dn	Dn	Dn	Up
AC0000	11,008K	A80000	10,752K	Dn	Up	Dn	Up	Dn	Dn	Dn	Dn
AD0000	11,072K	A90000	10,816K	Dn	Up	Dn	Dn	Up	Up	Up	Up
AE0000	11,136K	AA0000	10,880K	Dn	Up	Dn	Dn	Up	Up	Up	Dn
AF0000	11,200K	AB0000	10,944K	Dn	Up	Dn	Dn	Up	Up	Dn	Up
B00000	11,264K	AC0000	11,008K	Dn	Up	Dn	Dn	Up	Up	Dn	Dn
B10000	11,328K	AD0000	11,072K	Dn	Up	Dn	Dn	Up	Dn	Up	Up
B20000	11,392K	AE0000	11,136K	Dn	Up	Dn	Dn	Up	Dn	Up	Dn
B30000	11,456K	AF0000	11,200K	Dn	Up	Dn	Dn	Up	Dn	Dn	Up
B40000	11,520K	B00000	11,264K	Dn	Up	Dn	Dn	Up	Dn	Dn	Dn
B50000	11,584K	B10000	11,328K	Dn	Up	Dn	Dn	Dn	Up	Up	Up
B60000	11,648K	B20000	11,392K	Dn	Up	Dn	Dn	Dn	Up	Up	Dn
B70000	11,712K	B30000	11,456K	Dn	Up	Dn	Dn	Dn	Up	Dn	Up
B8000	11,776K	B40000	11,520K	Dn	Up	Dn	Dn	Dn	Up	Dn	Dn

BASE ADDRESS SWITCH TABLES

Memory Size/Address				Jumper Setting							
256K		512K		J12				J13			
B90000	11,840K	B50000	11,584K	Dn	Up	Dn	Dn	Dn	Dn	Up	Up
BA0000	11,904K	B60000	11,648K	Dn	Up	Dn	Dn	Dn	Dn	Up	Dn
BB0000	11,968K	B70000	11,712K	Dn	Up	Dn	Dn	Dn	Dn	Dn	Up
BC0000	12,032K	B80000	11,776K	Dn	Up	Dn	Dn	Dn	Dn	Dn	Dn
BD0000	12,096K	B90000	11,840K	Dn	Dn	Up	Up	Up	Up	Up	Up
BE0000	12,160K	BA0000	11,904K	Dn	Dn	Up	Up	Up	Up	Up	Dn
BF0000	12,224K	BB0000	11,968K	Dn	Dn	Up	Up	Up	Up	Dn	Up
C00000	12,288K	BC0000	12,032K	Dn	Dn	Up	Up	Up	Up	Dn	Dn
C10000	12,352K	BD0000	12,096K	Dn	Dn	Up	Up	Up	Dn	Up	Up
C20000	12,416K	BE0000	12,160K	Dn	Dn	Up	Up	Up	Dn	Up	Dn
C30000	12,480K	BF0000	12,224K	Dn	Dn	Up	Up	Up	Dn	Dn	Up
C40000	12,544K	C00000	12,288K	Dn	Dn	Up	Up	Up	Dn	Dn	Dn
C50000	12,608K	C10000	12,352K	Dn	Dn	Up	Up	Dn	Up	Up	Up
C60000	12,672K	C20000	12,416K	Dn	Dn	Up	Up	Dn	Up	Up	Dn
C70000	12,736K	C30000	12,480K	Dn	Dn	Up	Up	Dn	Up	Dn	Up
C80000	12,800K	C40000	12,544K	Dn	Dn	Up	Up	Dn	Up	Dn	Dn
C90000	12,864K	C50000	12,608K	Dn	Dn	Up	Up	Dn	Dn	Up	Up
CA0000	12,928K	C60000	12,672K	Dn	Dn	Up	Up	Dn	Dn	Up	Dn
CB0000	12,992K	C70000	12,736K	Dn	Dn	Up	Up	Dn	Dn	Dn	Up
CC0000	13,056K	C80000	12,800K	Dn	Dn	Up	Up	Dn	Dn	Dn	Dn
CD0000	13,120K	C90000	12,864K	Dn	Dn	Up	Dn	Up	Up	Up	Up
CE0000	13,184K	CA0000	12,928K	Dn	Dn	Up	Dn	Up	Up	Up	Dn
CF0000	13,248K	CB0000	12,992K	Dn	Dn	Up	Dn	Up	Up	Dn	Up
D00000	13,312K	CC0000	13,056K	Dn	Dn	Up	Dn	Up	Up	Dn	Dn
D10000	13,376K	CD0000	13,120K	Dn	Dn	Up	Dn	Up	Dn	Up	Up
D20000	13,440K	CE0000	13,184K	Dn	Dn	Up	Dn	Up	Dn	Up	Dn
D30000	13,504K	CF0000	13,248K	Dn	Dn	Up	Dn	Up	Dn	Dn	Up
D40000	13,568K	D00000	13,312K	Dn	Dn	Up	Dn	Up	Dn	Dn	Dn
D50000	13,632K	D10000	13,376K	Dn	Dn	Up	Dn	Dn	Up	Up	Up
D60000	13,696K	D20000	13,440K	Dn	Dn	Up	Dn	Dn	Up	Up	Dn
D70000	13,760K	D30000	13,504K	Dn	Dn	Up	Dn	Dn	Up	Dn	Up
D80000	13,824K	D40000	13,568K	Dn	Dn	Up	Dn	Dn	Up	Dn	Dn
D90000	13,888K	D50000	13,632K	Dn	Dn	Up	Dn	Dn	Dn	Up	Up
DA0000	13,952K	D60000	13,696K	Dn	Dn	Up	Dn	Dn	Dn	Up	Dn
DB0000	14,016K	D70000	13,760K	Dn	Dn	Up	Dn	Dn	Dn	Dn	Up
DC0000	14,080K	D80000	13,824K	Dn	Dn	Up	Dn	Dn	Dn	Dn	Dn
DD0000	14,144K	D90000	13,888K	Dn	Dn	Dn	Up	Up	Up	Up	Up
DE0000	14,208K	DA0000	13,952K	Dn	Dn	Dn	Up	Up	Up	Up	Dn
DF0000	14,272K	DB0000	14,016K	Dn	Dn	Dn	Up	Up	Up	Dn	Up
E00000	14,336K	DC0000	14,080K	Dn	Dn	Dn	Up	Up	Up	Dn	Dn
E10000	14,400K	DD0000	14,144K	Dn	Dn	Dn	Up	Up	Dn	Up	Up
E20000	14,464K	DE0000	14,208K	Dn	Dn	Dn	Up	Up	Dn	Up	Dn
E30000	14,528K	DF0000	14,272K	Dn	Dn	Dn	Up	Up	Dn	Dn	Up
E40000	14,592K	E00000	14,336K	Dn	Dn	Dn	Up	Up	Dn	Dn	Dn
E50000	14,656K	E10000	14,400K	Dn	Dn	Dn	Up	Dn	Up	Up	Up
E60000	14,720K	E20000	14,464K	Dn	Dn	Dn	Up	Dn	Up	Up	Dn
E70000	14,784K	E30000	14,528K	Dn	Dn	Dn	Up	Dn	Up	Dn	Up

BASE ADDRESS SWITCH TABLES

Memory Size/Address				Jumper Setting							
256K		512K		J12				J13			
E80000	14,848K	E40000	14,592K	Dn	Dn	Dn	Up	Dn	Up	Dn	Dn
E90000	14,912K	E50000	14,656K	Dn	Dn	Dn	Up	Dn	Dn	Up	Up
EA0000	14,976K	E60000	14,720K	Dn	Dn	Dn	Up	Dn	Dn	Up	Dn
EB0000	15,040K	E70000	14,784K	Dn	Dn	Dn	Up	Dn	Dn	Dn	Up
EC0000	15,104K	E80000	14,848K	Dn	Dn	Dn	Up	Dn	Dn	Dn	Dn
ED0000	15,168K	E90000	14,912K	Dn	Dn	Dn	Dn	Up	Up	Up	Up
EE0000	15,232K	EA0000	14,976K	Dn	Dn	Dn	Dn	Up	Up	Up	Dn
EF0000	15,296K	EB0000	15,040K	Dn	Dn	Dn	Dn	Up	Up	Dn	Up
F00000	15,360K	EC0000	15,104K	Dn	Dn	Dn	Dn	Up	Up	Dn	Dn
F10000	15,424K	ED0000	15,168K	Dn	Dn	Dn	Dn	Up	Dn	Up	Up
F20000	15,488K	EE0000	15,232K	Dn	Dn	Dn	Dn	Up	Dn	Up	Dn
F30000	15,552K	EF0000	15,296K	Dn	Dn	Dn	Dn	Up	Dn	Dn	Up
F40000	15,616K	F00000	15,360K	Dn	Dn	Dn	Dn	Up	Dn	Dn	Dn
F50000	15,680K	F10000	15,424K	Dn	Dn	Dn	Dn	Dn	Up	Up	Up
F60000	15,744K	F20000	15,488K	Dn	Dn	Dn	Dn	Dn	Up	Up	Dn
F70000	15,808K	F30000	15,552K	Dn	Dn	Dn	Dn	Dn	Up	Dn	Up
F80000	15,872K	F40000	15,616K	Dn	Dn	Dn	Dn	Dn	Up	Dn	Dn
F90000	15,936K	F50000	15,680K	Dn	Dn	Dn	Dn	Dn	Dn	Up	Up
FA0000	16,000K	F60000	15,744K	Dn	Dn	Dn	Dn	Dn	Dn	Up	Dn
FB0000	16,064K	F70000	15,808K	Dn	Dn	Dn	Dn	Dn	Dn	Dn	Up
FC0000	16,128K	F80000	15,872K	Dn	Dn	Dn	Dn	Dn	Dn	Dn	Dn

APPENDIX B - DISCUSSION OF ENGINEERING SPECIFICATIONS

MSR Series Access Time Specification.

With 120 ns RAMS installed, the access time is typically 120 to 125 nanoseconds measured at the bus. Worst case access time is 166 nanoseconds over the entire 0 to 70 degree centigrade temperature range using a 4.75 to 5.25 volt power range after regulation. Cycle time is less than 290 ns, allowing full speed operation in high speed environments.

It should be mentioned that most manufacturers use their typical-case figures for advertising purposes. In many respects this is an indication of how you may expect a memory board to perform. It does not, however, tell the entire story.

The MSR's typical-case values are derived from observing the worst case times in a large sample of production boards exposed to various environments. The absolute worst-case values given above are calculated using the worst-case figures supplied by the IC manufacturers. These figures are guaranteed values for extreme cases (ie: low voltage, high temperatures and board designs with a high fan out on every device). In other words, the maximum values presented for the MSR are extremely conservative.

TECHNICAL DISCUSSION OF SPECIFICATIONS

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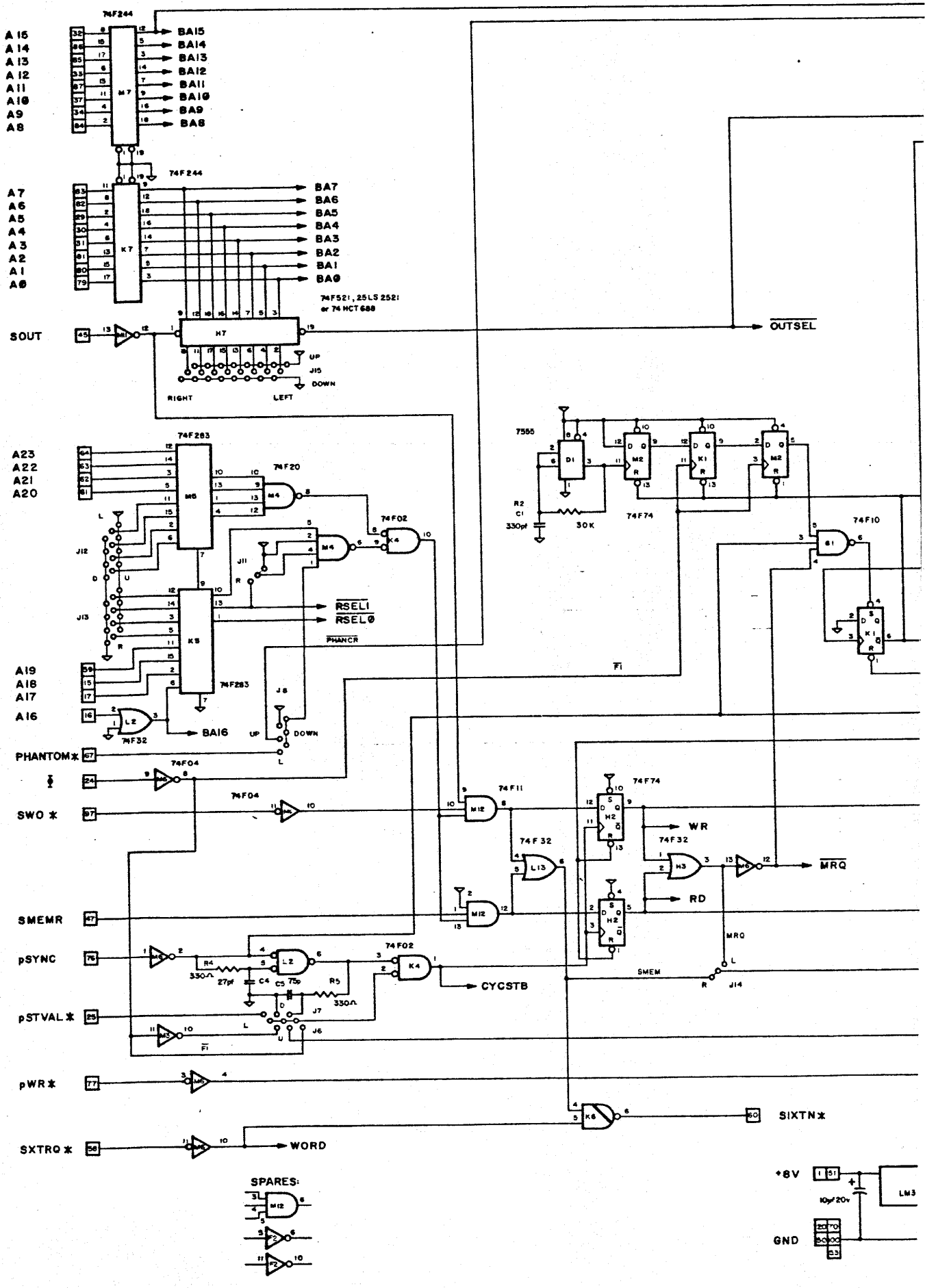
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R2
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30K
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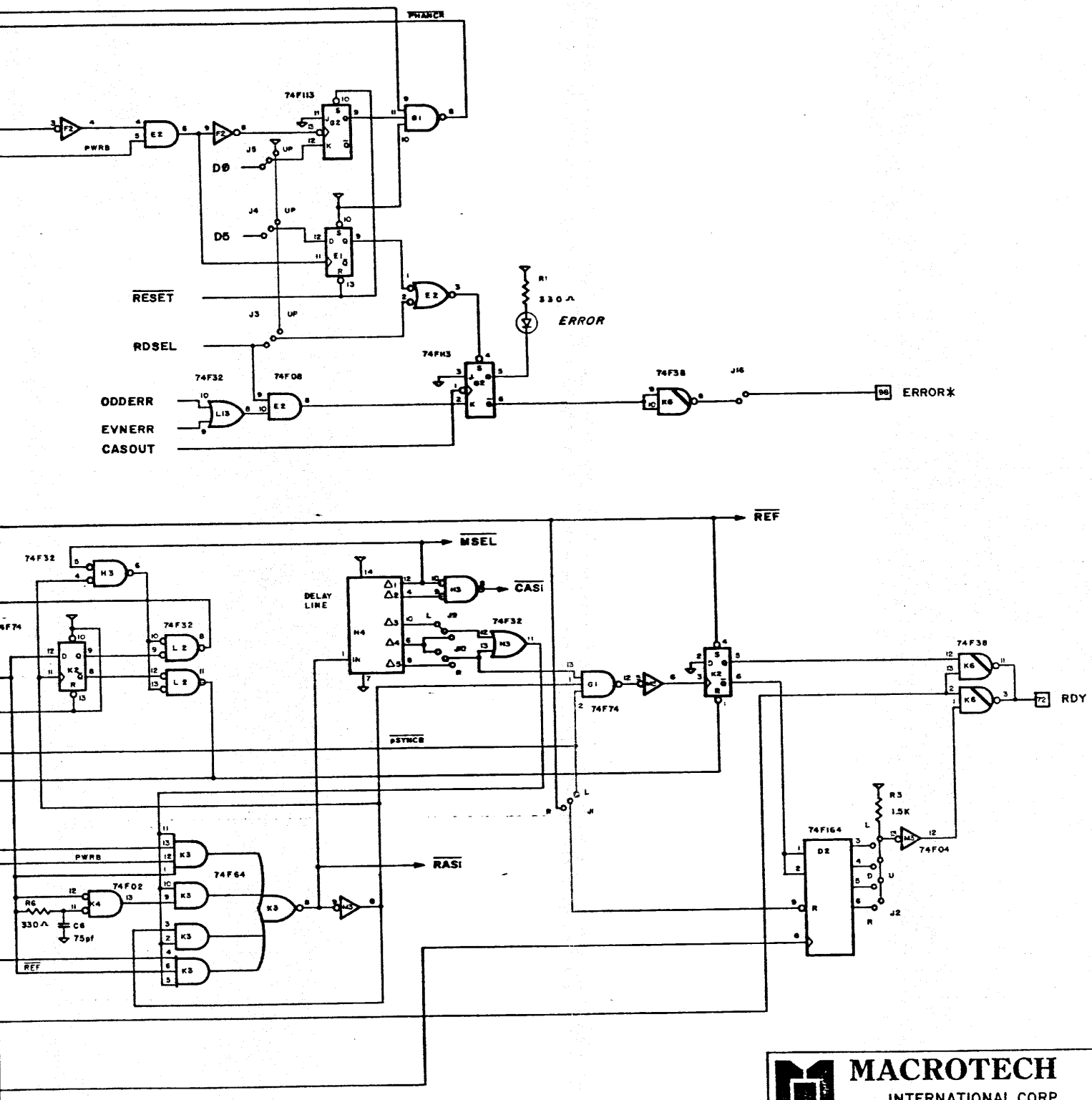
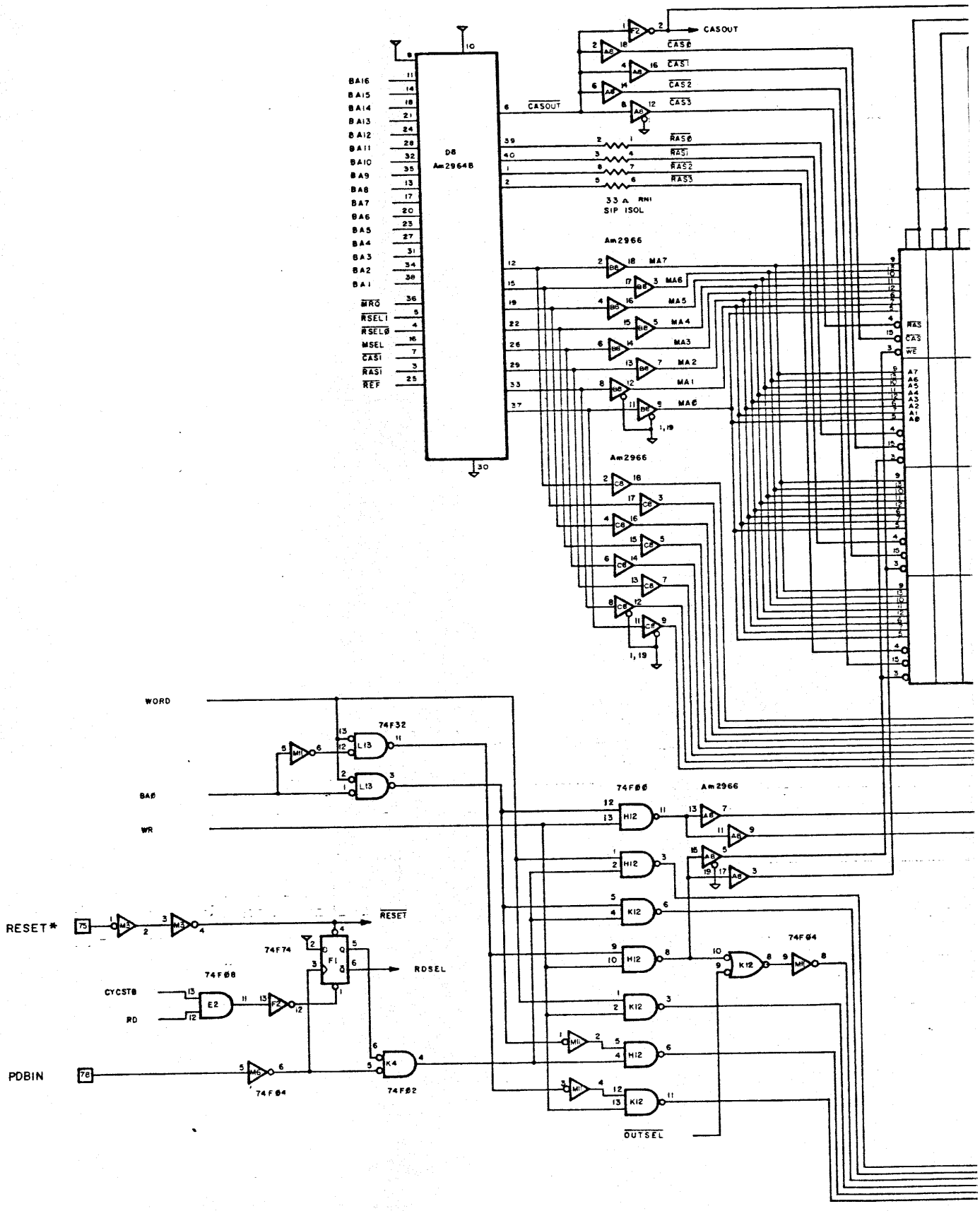


MACROTECH
INTERNATIONAL CORP.

MSR 512K DYNAMIC MEMORY BOARD
FOR THE S-100 BUS

DESIGNED: HOWARD OGLE
DRAWN: C. R. BRYAN III

V1.0
07NOV84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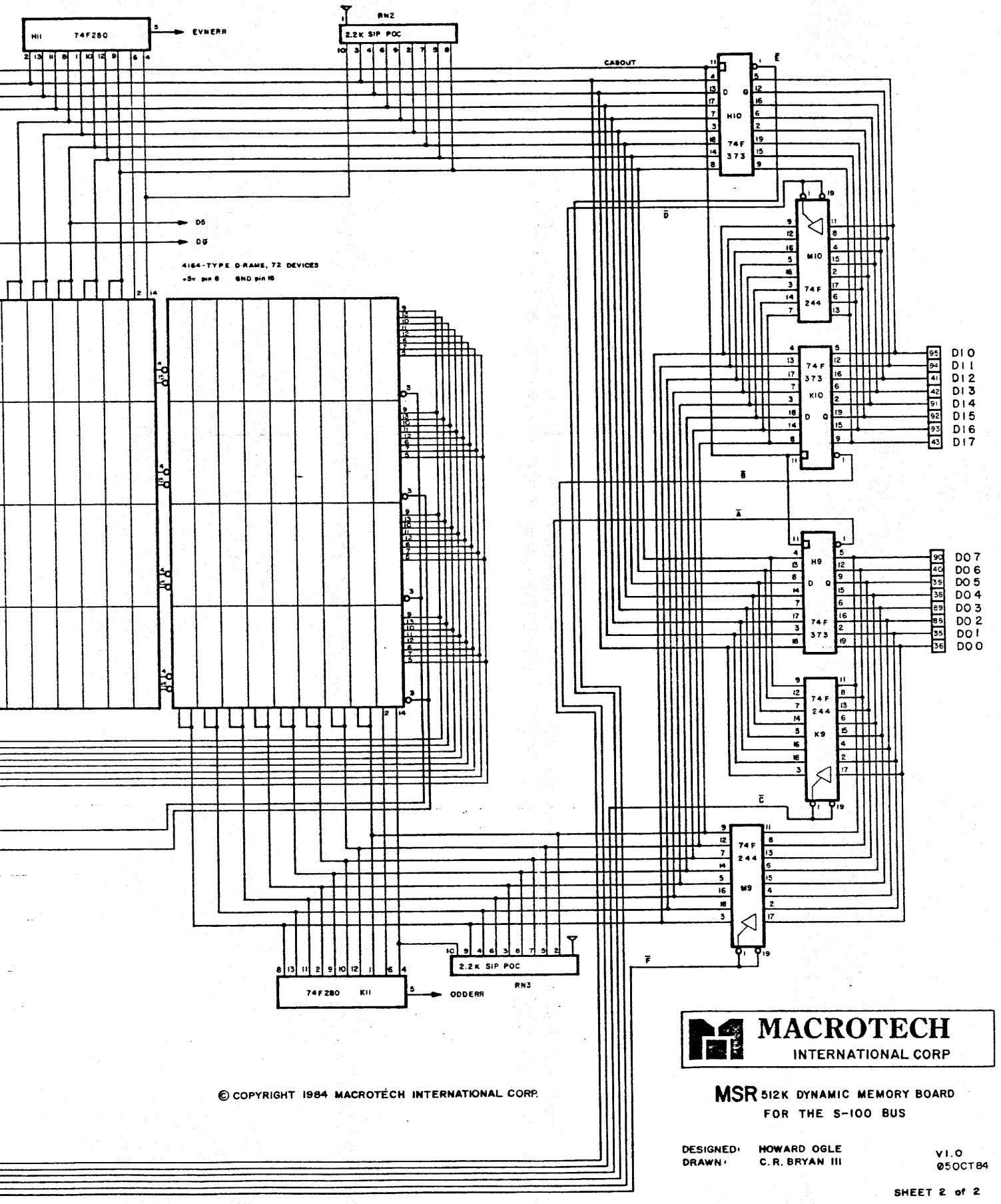

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