1.0 INTRODUCTION - MACROTECH ADDRESSING CONCEPTS

The purpose of this section is to acquaint the user with the flexible addressing capabilities of the Macrotech 512-ST Static Ram Memory Board. Since certain terminologies used in this section may be new or perhaps vary from your present usage, the glossary at the end of this manual provides definitions of the intended meaning of terms used in this text. Before reading on, please take a moment to scan the glossary and familiarize yourself with the terminologies presented here.

1.1 PHYSICAL ADDRESS GENERATION

Any given data byte or word in the 512-ST memory array has a single unique 24-bit physical address. This address may be generated by the CPU system with 24-bit Extended Addressing, or by the 512-ST when used in a system with 16-bit Standard Addressing.
The Physical Address holds the same relationship to the memory array regardless of the address mode employed, and is thus the common basis for address generation in any functional mode. There are two components to the generated physical address:

1. Board select bits: PA23-PA17
2. Byte/word select bits: PA16-PA00

The 512-ST has three basic functional addressing modes. All modes are designed to provide the required 24-bit physical array address. At any moment in time, one of the three addressing modes will be in operation. The three functional addressing modes are:

1. **24-bit (extended) mode** - Where the physical address is equal to the 24-bit logical address. (PA23-PA00 = LA23-LA00).

2. **16-bit (standard) pass mode** - A submode of map mode addressing. Invoked at power-up or reset to provide 64k of memory to the system for initialization. Pass mode automatically maps the lower 64k of the selected board to be active in this mode. In the selected 512-ST, the upper eight bits (PA23-PA16) of the generated physical address are forced to logical zeroes and the remaining sixteen physical address bits (PA15-PA00) are passed directly from the logical address bus (LA15-LA00) when pass mode addressing is invoked.

3. 16-bit (standard) map mode - In map mode addressing, the upper twelve physical address bits (PA23-PA12) are generated by the map register outputs (MO23-MO12), and the lower twelve physical address bits (PA11-PA00) are passed to the memory array directly from the logical address bus (LA11-LA00). Note that the term "Standard" in this context refers to the IEEE/696 definition of a 16-bit address bus, and that mapped (M3) addressing is actually an optional feature of the 512-ST.

24-BIT ADDRESSING MODE

This addressing mode option is in compliance with the IEEE/696 Extended Addressing specifications. It is used with systems which provide an address bus of more than 16 bits (i.e. 80286, 68000, 8086, 8088, etc.). Some of the eight bit systems are also equipped to handle extended addressing, and will allow the use of the 24-bit addressing mode of the 512-ST. It should be noted however, that most of the conventional "extended" addressing schemes for the eight bit processors are not designed to make as efficient use of memory as Macrotech's M3 Memory Mapped Addressing. The user is advised to study the differences in concepts to determine the optimal configuration for the target system.

In the 24-bit addressing mode, logical address bits (LA23-LA00) from the bus are unmodified by the 512-ST and are used to directly address the physical memory array (PA23-PA00).

16-BIT M3 MEMORY MAPPED ADDRESSING - GENERAL THEORY

The Macrotech M3 Memory Mapping architecture is a powerful tool designed to permit addressing of up to 16 Megabytes of memory space in a system incorporating a Standard (16-bit) address bus.
The M3 concept uses the four most significant bits of the sixteen logical address bits from the bus to address a pointer (mapping register) into the physical array. Sixteen twelve-bit registers provided on board the 512-ST establish a register for each 4k bank of the 64k logical address bus. Each register is addressed by the 4 most significant Logical Address bits - (LA15-LA12), and the resulting twelve-bit map register output (MO23-MO12) forms a pointer into any 4k bank of the Physical Array (PA23-PA12). The Logical to Physical path for Map Mode Addressing is shown in Figures 1.3 and 1.4.

The M3 mapping registers (mmr0 - mmrf), are loaded through I/O as 16 individual contiguous write-only I/O ports, selected by the user at any 16 byte boundary (n0 - nf). All M3 boards in the system should utilize the same I/O address space for effective memory management. Each map register (mmr0-mmrf) contains the same value as the respective register in every board in the system.
The actual physical address, PA23-PA00, is derived from the Map Address bits MO23-MO12, and Logical Address bits LA11-LA00. Board Select* is a function of Map Address bits MO23-MO17 in this mode, and the remaining bits (MO16-MO12 and LA11-LA00) directly address the physical memory array of the selected board.

A seventeenth write-only I/O port, the "MAX" register, is provided to assert the four most significant bits of the twelve-bit map register values. Use of this port is not necessary in applications where a megabyte or less memory is installed in the target system, addressed within the first megabyte of memory space (000000-0fffffh). When this option is selected, the four most significant map data bits are supplied through a latch which is addressed by the 17th port. These four bits (MD23-MD20) are cleared to zero at power-up, reset, or when 20-bit translate mode is selected.

20/24 BIT ADDRESS M3 TRANSLATION

The M3 addressing option provides the capability of translating a sixteen bit logical address to either a 20-bit (one megabyte maximum) or a 24-bit (sixteen megabyte) physical address at the users option. The criteria for determining the proper selection are as follows:

1. 20-bit translation is used when the total system memory will be located within the lowermost one megabyte range of memory address space. The four most significant bits of the 12-bit value written to the map registers are automatically set to zero when 20-bit translation is selected.
The principle advantage of this mode is that each map register is loaded with a single byte from the data-out bus and the automatically zeroed upper four bits require no software overhead. Since the seventeenth port is not used in this mode, its address can be used elsewhere in the system if needed.

2. 24-bit translation is used when the total system memory is greater than one megabyte, **or** when some or all of that memory is located above the boundary of tne first megabyte of address space.

A four bit value representing the megabyte range to be addressed is presented to the four most significant bits of the mapping registers through a 4-bit latch, and all **subsequent** map register loads will include that latched megabyte range value until a new value is written into the latch.
Once the desired value is written into the latch, map register loading is identical to loading in the 20-bit translate mode. The latched 4-bit megabyte range value and the 8-bit register load value are combined to form a 12-bit full map register load value.

Regardless of the translation mode employed (20 or 24 bit), all 12 bits are loaded into each of the 16 mmr's. The only difference between the two modes is that in 20-bit translate mode the four most significant bits are always forced to zero, limiting the total addressing range to the lowermost one megabyte, while 24-bit translate mode permits addressing over the entire 16 megabyte range.

MAPPING REGISTER I/O SELECTION

Sixteen I/O ports are required for M3 addressing when the 20-bit translate mode is selected; seventeen ports are required for the 24-bit translate mode. In either mode, addressing is contiguous and a four bit setting of the base I/O address upper nibble is the only selection required. The sixteen map registers are always addressed by n0-nf, where n is the selected map register base address. When 24-bit translate mode is selected, the seventeenth (latch) port address is determined by the on-board logic as follows:

a. If the selected map register base address is an even value, the seventeenth port address will be located at base+16.
Example: I/O base address set to 4 (40-4fh). In this case the seventeenth port address assignment will be 50h (40h + 16 = 50h).

b. If the base address selection is an odd value, the seventeenth port address will be located at base-1.
Example: I/O base address set to 3 (30-3fh). The seventeenth port assignment will be 2fh (30h - 1 = 2fh).

Note that this structure uses a contiguous block of I/O address space in either an even or odd I/O address selection. Also note that when 20-bit translation is utilized, the seventeenth port is not used by the 512-ST and the address is free to be used elsewhere in the system if desired.

In the 24-bit addressing mode, logical address bits (LA23-LA00) from the system bus are unmodified by the 512-ST and are used to directly address the physical memory array (PA23-PA00).

1.4 M3 MEMORY MAPPED ADDRESSING - PASS MODE

This mode is automatically invoked at power-up or system reset when the M3 addressing mode is selected. Only one board in the system should be set up to be active in pass mode. (See figure 1.2 - pass mode address path.) In conventional applications, the zero level board (000000-07ffffh) will be set to be active for pass mode addressing.
In pass mode addressing, the lower 64k of the active 512-ST is available to the system. Physical address bits PA23-PA16 are all forced to logic zero. Logical address bits LA15-LA00 are passed unmodified to the physical array (PA15-PA00). The immediate availability of the lowermost 64k of system memory in pass mode allows the programmer to initialize the mapping registers (mmr0 - mmrf).
Three Golden Rules must be observed in the implementation of Map Register initialization:

RULE #1 All sixteen mapping registers must be initialized. Unwritten registers will contain random data at power up and unpredictable results will occur if this rule is ignored.

RULE #2 The initial map load should be a one to one duplication of pass mode addressing i.e. mmr0=00, mmr1=01,....mmrf=0f etc. This practice assures a smooth transition from pass mode addressing to map mode addressing with no surprises.

RULE #3 The last mapping register to be loaded in the initialization sequence must be the the highest order register - mmrf. **It is the act of loading this register that switches addressing modes from pass mode to map mode.** All subsequent memory transactions will be accessed through the mapping registers once mmrf is loaded.
This is the point of no return. Map mode addressing will remain in effect until the system is powered up/down or a system reset occurs.

The following figures (figures 1.1 - 1.5) and the chart (table 1.1) illustrate the various sources and paths for logical to physical address translation for each of the four addressing modes of the 512-ST.

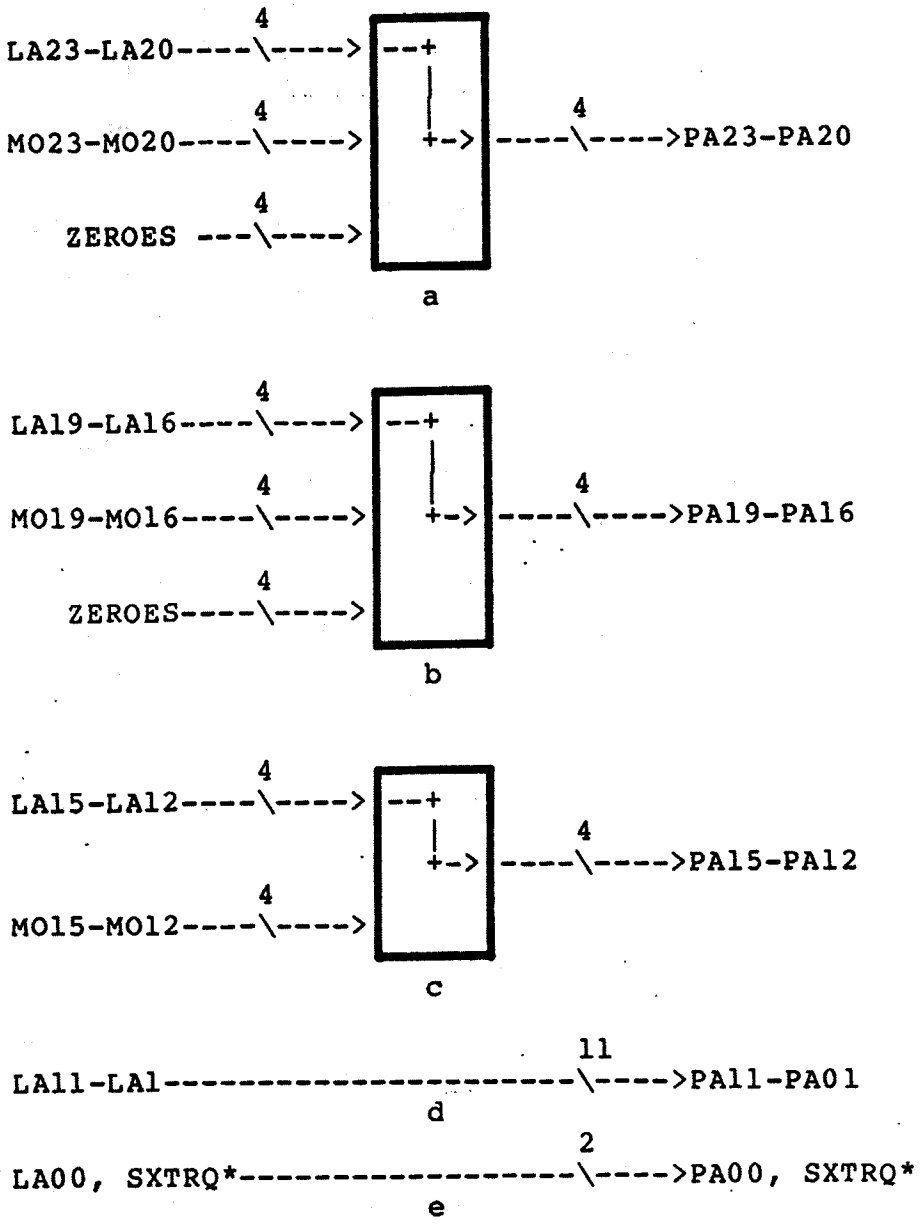
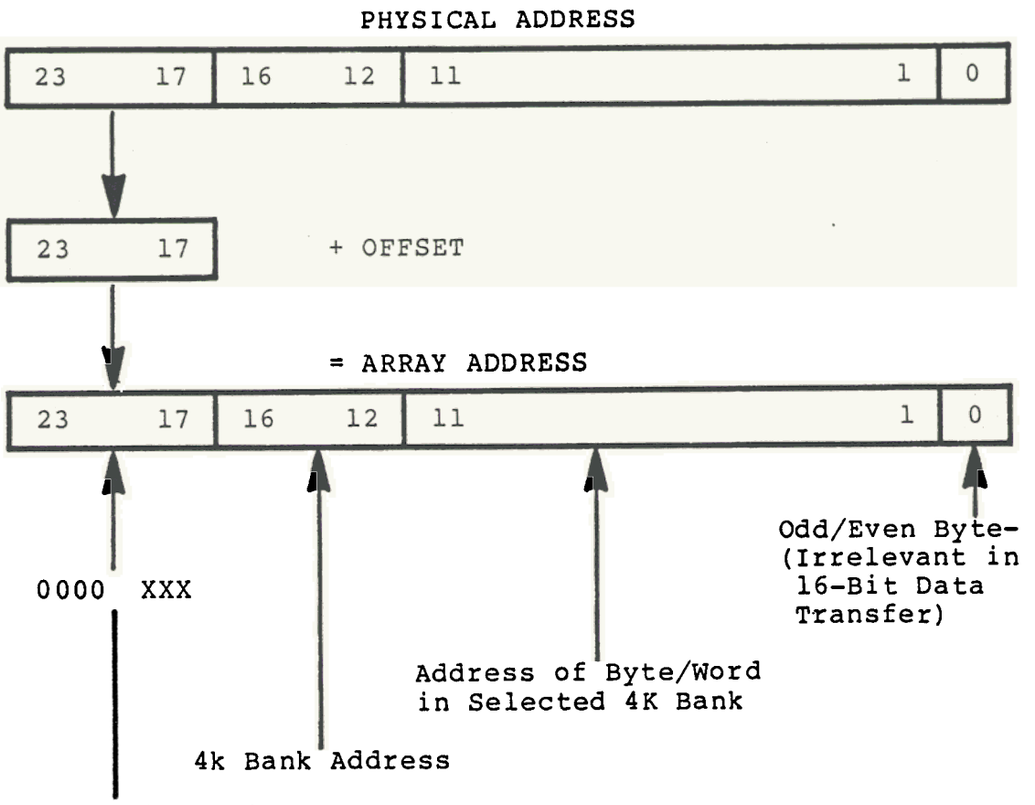


FIGURE 1.1 24-BIT ADDRESS PATH

Physical Address Source:

Group a: PA23-20	Group b: PA19-16	Group c: PA15-12	Group d: PA11-01	Group e: PA00,SXTRQ*
LA23-20	LA19-16	LA15-12	LA11-01	LA00,SXTRQ*



Note: XXX denotes 000 to highest 128k block available:

XXX	Range (Dec)	Range (Hex)
000 =	0K - 128K	000000 - 01FFFFH
001 =	128K - 256K	020000 - 03FFFFH
010 =	256K - 384K	040000 - 05FFFFH
011 =	384K - 512K	060000 - 07FFFFH

FIGURE 1.5 ARRAY ADDRESS GENERATION

2.0 EXTENDED ADDRESSING (24-BIT)

2.1 USE

The 512-ST is fully compatible with the 24-bit extended addressing specified in the IEEE/696 and implemented in all of the new generation of 16-bit and many of the 8-bit S100 computer systems. Jumper strapping options permit each 512-ST to be located on any 128k boundary in the defined 16 megabyte memory space.

2.2 INSTALLATION

When extended addressing is to be used, it must be selected by jumper J2C. The address range selection of the board in the 16M address space must be specified via the J2D-F and J3A-D jumpers as shown in table 2.1. This table also shows that no other address related options are applicable. The relationship between the individual jumpers and the set of possible memory address range selections is shown in table 2.2. Note that jumper blocks J2B, J4A-D and J5D are not used in the extended addressing mode and the positioning of these jumpers will not affect the address selection or operation in this mode.

Jumper	Loc'n	Address Line	Installed Left	Installed Right	Description & Comments
J4-D	K1	A7	A7=1	A7=0	Not used in
J4-C		A6	A6=1	A6=0	Extended (24-bit)
J4-B		A5	A5=1	A5=0	Addressing Mode
J4-A		A4	A4=1	A4=0	
J3-A	H1	A23	OFS23=1	OFS23=0	Board Address
J3-D		A22	OFS22=1	OFS22=0	Select. Defines
J3-C		A21	OFS21=1	OFS21=0	the origin of the
J3-B		A20	OFS20=1	OFS20=0	memory on this
J2-D		A19	OFS19=1	OFS19=0	board within the
J2-F		A18	OFS18=1	OFS18=0	16M addressable
J2-E		A17	OFS17=1	OFS17=0	memory space.

Table 2.1 - Address Jumper Definitions
Extended Addressing

512-ST Board Base Address		-------- OFFSET JUMPER SETTINGS ----------						
Hex'	decimal	ofs23 J3A	ofs22 J3D	ofs21 J3C	ofs20 J3B	ofs19 J2D	ofs18 J2F	ofs17 J2E
000000	0K	R	R	R	R	R	R	R
020000	128K	L	L	L	L	L	L	L
040000	256K	L	L	L	L	L	L	R
060000	384K	L	L	L	L	L	R	L
080000	512K	L	L	L	L	L	R	R
0A0000	640K	L	L	L	L	R	L	L
0C0000	768K	L	L	L	L	R	L	R
0E0000	896K	L	L	L	L	R	R	L
100000	1,024K	L	L	L	L	R	R	R
120000	1,152K	L	L	L	R	L	L	L
140000	1,280K	L	L	L	R	L	L	R
160000	1,408K	L	L	L	R	L	R	L
180000	1,536K	L	L	L	R	L	R	R
1A0000	1,664K	L	L	L	R	R	L	L
1C0000	1,792K	L	L	L	R	R	L	R
1E0000	1,920K	L	L	L	R	R	R	L
200000	2,048K	L	L	L	R	R	R	R
220000	2,176K	L	L	R	L	L	L	L
240000	2,304K	L	L	R	L	L	L	R
260000	2,432K	L	L	R	L	L	R	L
280000	2,560K	L	L	R	L	L	R	R
2A0000	2,688K	L	L	R	L	R	L	L
2C0000	2,816K	L	L	R	L	R	L	R
2E0000	2,944K	L	L	R	L	R	R	L
300000	3,072K	L	L	R	L	R	R	R
320000	3,200K	L	L	R	R	L	L	L
340000	3,328K	L	L	R	R	L	L	R
360000	3,456K	L	L	R	R	L	R	L
380000	3,584K	L	L	R	R	L	R	R
3A0000	3,712K	L	L	R	R	R	L	L
3C0000	3,840K	L	L	R	R	R	L	R
3E0000	3,968K	L	L	R	R	R	R	L

Table 2.2.1 - Board Address Selection

Note: "L" indicates jumper installed toward left of board
"R" indicates jumper installed toward right (away from regulator)
K = 1024

512-ST Board Base Address		OFFSET JUMPER SETTINGS						
Hex'	decimal	ofs23 J3A	ofs22 J3D	ofs21 J3C	ofs20 J3B	ofs19 J2D	ofs18 J2F	ofs17 J2E
400000	4,096K	L	L	R	R	R	R	R
420000	4,224K	L	R	L	L	L	L	L
440000	4,352K	L	R	L	L	L	L	R
460000	4,480K	L	R	L	L	L	R	L
480000	4,608K	L	R	L	L	L	R	R
4A0000	4,736K	L	R	L	L	R	L	L
4C0000	4,864K	L	R	L	L	R	L	R
4E0000	4,992K	L	R	L	L	R	R	L
500000	5,120K	L	R	L	L	R	R	R
520000	5,248K	L	R	L	R	L	L	L
540000	5,376K	L	R	L	R	L	L	R
560000	5,504K	L	R	L	R	L	R	L
580000	5,632K	L	R	L	R	L	R	R
5A0000	5,760K	L	R	L	R	R	L	L
5C0000	5,888K	L	R	L	R	R	L	R
5E0000	6,016K	L	R	L	R	R	R	L
600000	6,144K	L	R	L	R	R	R	R
620000	6,272K	L	R	R	L	L	L	L
640000	6,400K	L	R	R	L	L	L	R
660000	6,528K	L	R	R	L	L	R	L
680000	6,656K	L	R	R	L	L	R	R
6A0000	6,784K	L	R	R	L	R	L	L
6C0000	6,912K	L	R	R	L	R	L	R
6E0000	7,040K	L	R	R	L	R	R	L
700000	7,168K	L	R	R	L	R	R	R
720000	7,296K	L	R	R	R	L	L	L
740000	7,424K	L	R	R	R	L	L	R
760000	7,552K	L	R	R	R	L	R	L
780000	7,680K	L	R	R	R	L	R	R
7A0000	7,808K	L	R	R	R	R	L	L
7C0000	7,936K	L	R	R	R	R	L	R
7E0000	8,064K	L	R	R	R	R	R	L

Table 2.2.2 - Board Address Selection

Note: "L" indicates jumper installed toward left of board
"R" indicates jumper installed toward right (away from regulator)
K = 1024

512-ST Board Base Address		OFFSET JUMPER SETTINGS						
Hex'	decimal	ofs23 J3A	ofs22 J3D	ofs21 J3C	ofs20 J3B	ofs19 J2D	ofs18 J2F	ofs17 J2E
800000	8,192K	L	R	R	R	R	R	R
820000	8,320K	R	L	L	L	L	L	L
840000	8,448K	R	L	L	L	L	L	R
860000	8,576K	R	L	L	L	L	R	L
880000	8,704K	R	L	L	L	L	R	R
8A0000	8,832K	R	L	L	L	R	L	L
8C0000	8,960K	R	L	L	L	R	L	R
8E0000	9,088K	R	L	L	L	R	R	L
900000	9,216K	R	L	L	L	R	R	R
920000	9,344K	R	L	L	R	L	L	L
940000	9,472K	R	L	L	R	L	L	R
960000	9,600K	R	L	L	R	L	R	L
980000	9,728K	R	L	L	R	L	R	R
9A0000	9,856K	R	L	L	R	R	L	L
9C0000	9,984K	R	L	L	R	R	L	R
9E0000	10,112K	R	L	L	R	R	R	L
A00000	10,240K	R	L	L	R	R	R	R
A20000	10,368K	R	L	R	L	L	L	L
A40000	10,496K	R	L	R	L	L	L	R
A60000	10,624K	R	L	R	L	L	R	L
A80000	10,752K	R	L	R	L	L	R	R
AA0000	10,880K	R	L	R	L	R	L	L
AC0000	11,008K	R	L	R	L	R	L	R
AE0000	11,136K	R	L	R	L	R	R	L
B00000	11,264K	R	L	R	L	R	R	R
B20000	11,392K	R	L	R	R	L	L	L
B40000	11,520K	R	L	R	R	L	L	R
B60000	11,648K	R	L	R	R	L	R	L
B80000	11,776K	R	L	R	R	L	R	R
BA0000	11,904K	R	L	R	R	R	L	L
BC0000	12,032K	R	L	R	R	R	L	R
BE0000	12,160K	R	L	R	R	R	R	L

Table 2.2.3 - Board Address Selection

Note: "L" indicates jumper installed toward left of board
"R" indicates jumper installed toward right (away from regulator)
K = 1024

512-ST Board Base Address		-------- OFFSET JUMPER SETTINGS ----------						
Hex'	decimal	ofs23 J3A	ofs22 J3D	ofs21 J3C	ofs20 J3B	ofs19 J2D	ofs18 J2F	ofs17 J2E
C00000	12,288K	R	L	R	R	R	R	R
C20000	12,416K	R	R	L	L	L	L	L
C40000	12,544K	R	R	L	L	L	L	R
C60000	12,672K	R	R	L	L	L	R	L
C80000	12,800K	R	R	L	L	L	R	R
CA0000	12,928K	R	R	L	L	R	L	L
CC0000	13,056K	R	R	L	L	R	L	R
CE0000	13,184K	R	R	L	L	R	R	L
D00000	13,312K	R	R	L	L	R	R	R
D20000	13,440K	R	R	L	R	L	L	L
D40000	13,568K	R	R	L	R	L	L	R
D60000	13,696K	R	R	L	R	L	R	L
D80000	13,824K	R	R	L	R	L	R	R
DA0000	13,952K	R	R	L	R	R	L	L
DC0000	14,080K	R	R	L	R	R	L	R
DE0000	14,208K	R	R	L	R	R	R	L
E00000	14,336K	R	R	L	R	R	R	R
E20000	14,464K	R	R	R	L	L	L	L
E40000	14,592K	R	R	R	L	L	L	R
E60000	14,720K	R	R	R	L	L	R	L
E80000	14,848K	R	R	R	L	L	R	R
EA0000	14,976K	R	R	R	L	R	L	L
EC0000	15,104K	R	R	R	L	R	L	R
EE0000	15,232K	R	R	R	L	R	R	L
F00000	15,360K	R	R	R	L	R	R	R
F20000	15,488K	R	R	R	R	L	L	L
F40000	15,616K	R	R	R	R	L	L	R
F60000	15,744K	R	R	R	R	L	R	L
F80000	15,872K	R	R	R	R	L	R	R
FA0000	16,000K	R	R	R	R	R	L	L
FC0000	16,128K	R	R	R	R	R	L	R
FE0000	16,256K	R	R	R	R	R	R	L

Table 2.2.4 - Board Address Selection

Note: "L" indicates jumper installed toward left of board
"R" indicates jumper installed toward right (away from regulator)

K = 1024

Jumper	Loc'n	Signal or Line	Active Position	Description & Comments
J2C	G1	Addr. Mode	Left (Right	Extended 24-bit Addressing Standard 16-bit Addressing)
J2B	G1	DMA Mode	don't care	24-bit DMA Addressing

Table 2.3 Address Mode Selection
Extended Addressing

3.0 STANDARD ADDRESSING (16-BIT)

3.1 MACROTECH MEMORY MAPPING (M3)

"M3 " denotes the powerful, proprietary Macrotech Memory Mapping architecture. M3 is a translation mechanism which permits effective use of a large memory space - up to 16 megabytes - by processors able to address only 64k of memory. Each 512-ST contains eight times the memory normally addressed by a Z-80, 8085, or other processor using the standard 16-bit IEEE/696 addressing mode; up to thirty-two standard addressing 512-ST boards may reside in a single system. M3 allows the most flexible use possible of this much memory by a standard-addressing microprocessor.

Each 512-ST contains sixteen "8-bit" memory mapping registers - mmr0-mmrf (as previously discussed, they are actually twelve bits wide, with the 17th register providing the upper four bits when they are loaded). These registers dynamically translate each 16-bit logical address on the bus into a single 24-bit address in the sixteen megabyte physical memory space. The mapping registers themselves are written to by treating each as an independent I/O device.

For all M3 boards in a system, the memory mapping registers are used as if only a single set of 16 such registers existed. For example, any time mmr0 is accessed (to be loaded), it is accessed (written to) on **all** 512-ST memory boards simultaneously. For accessing, these registers are assigned to a contiguous block of 16 I/O addresses of the form n0 through nf, where n(=0,1,---,f) represents the upper nibble of an otherwise unused sequence of port addresses. By setting "n" on each board to the **same** value, the registers on all boards are loaded simultaneously. Thus, mmr0 on all boards will always contain the same value, and similarly for mmr1,mmr2,----mmrf.

Each memory mapping register mmri (i=0,---,f), contains a twelve-bit field uniquely identifying one of the possible 4k banks in the useable 16M physical memory space. Together, all of the mmr registers thus identify 16 such banks, thereby defining a 64k logical memory space addressed by the 16-bit address on the bus.

To effect the translation from a logical to a physical address, the four most significant address bits on the bus (A15, A14, A13 and A12) are used by each M3 board as the 4-bit address of one of the memory mapping registers. The low order twelve bits on the bus, A11 - A0 are appended to the twelve bits from the selected mmr to form a 24-bit physical address, A23 - A0. When the M3 boards are properly installed, **only one board will actually contain the derived physical address.** The containing board will access the addressed memory location exactly as if both a 24-bit address had been presented on the bus **and** 24-bit addressing had been specified.

When the 16M physical space is not fully occupied, one or more mmr's can be loaded with a value for a non-existent 4k page, causing the bus to address a region that has no memory. This capability is useful in systems with fixed ROM memory that cannot be "phantomed" out of the 64k memory space. Since no M3 board has memory in that 4K gap, no M3 board will respond to the access in collision with the ROM.

3.1.1 START-UP IN PASS MODE

Following both "Power up" and "Reset" conditions, it must be assumed that the initial values of the mmr are not meaningful. If desired, one M3 board can be set to pass the 16-bit addresses from the bus directly to the memory address decoding logic, bypassing the mmr (but not the address offset adders) and restricting access to only the first 64k of memory. Except where this option is elected for **one** board, all M3 boards must be set to **not** pass through the 16-bit address from the bus.
Selection of the Pass mode provides the operating system with known physical memory during the initial power-up phase and subsequent system resets. If the pass mode is not enabled on a board, then power-up or reset causes its memory to be inaccessible until all the mmr are safely loaded with the initial map values. Whether the board is set to be enabled or disabled following a reset or power-up sequence, normal operation is invoked when the high-order memory mapping register (mmrf) is loaded. Note that **all** sixteen mmr must be initialized in order to assure reliable operation in mapped addressing mode.

3.2 INSTALLATION

3.2.1 BOARD ADDRESS RANGE SELECT

Jumpers J2D-F and J3A-D define the memory address range of the 512-ST board, referenced to a 256 kbyte or 512 kbyte boundary in the 16 megabyte addressable memory space, as shown in table 3.1. As in extended addressing mode, these jumpers are plug-programmed with an address offset to which is added the 24-bit physical address (in this case provided by the M3 translation mechanism). Board-select occurs when all bits in the resultant sum are zeroes except for those bits which specify locations within the board's RAM array.

3.2.2 SELECTION OF I/O ADDRESS FOR MEMORY MAPPING REGISTERS

The 512-ST's I/O requirements are different for the three main operating modes.

In Extended (24-bit) Addressing Mode, the board needs no I/O address space, because no mapping registers are used.

In 20-bit Map Mode (used when all M3 memory is within the first megabyte of extended address space), the 512-ST uses a contiguous block of 16 addresses, n0 through nf (n = 0, 1,---, f) for the standard set of 8-bit I/O addresses defined in the IEEE/696. The most significant nibble of the assigned address, "n" is selected on the board via jumpers J3-D, -C, -A and -B per the following rules:

a. All M3 memory boards in the system must have same mmr I/O address block selected.

b. No other I/O output device or register in the system can share any of the block of 16 mmr I/O addresses.

The I/O address bit versus jumper relationship is given in table 3.1.

In 24-bit Map Mode (used when there is M3 memory in extended addresses above the first megabyte), the 512-ST uses a total of 17 I/O addresses, the seventeenth one being the "MAX" register.

As in 20-bit Map Mode, the sixteen mapping registers plus the MAX register must be the only I/O output devices to occupy their contiguous 17-port I/O block. (None of the 17 registers will respond to an I/O read.)

Addressing of the MAX register is automatic. The MAX register will be appended to the top of the 16-port block if the upper nibble of the port block's addresses is even; to the bottom if odd. This eliminates port wraparound, but it must be taken into consideration in assigning the block's port addresses. If mmr0 is assigned port# 10, the MAX register is at port# 0F; if mmr0 is at port# 00, the MAX register will respond to I/O writes at port #11.

3.2.3 SELECTION OF BOARD IN PASS MODE ON POWER-UP OR RESET

As described in 3.1 above, either none or one M3 board in a system may be set to provide an unmapped 64k of memory for use by the system during initialization following a power-up or reset sequence. On the 512-ST, jumper J5-D is used for this purpose. When jumper J5-D is installed leftwards on the chosen M3 board, that board will respond to all memory accesses until the system leaves Pass mode. Its lowest 64k of memory will automatically respond directly to 16-bit addressing, bypassing the mmr's.

Only one M3 board in the system should be enabled in this way, and then only if no other board in the system is going to serve as memory for initial system operations.

The address offset adders are not bypassed in Pass mode, so the enabled board will not respond unless its offset jumpers are configured to a base address of 0h (covering the lowest 64k of address space).

If jumper J5-D is installed in the "left" position, the power-up or reset sequence establishes the board as **disabled** and the board will not respond to access requests in Pass mode.

Whether the board is enabled or disabled in Pass mode, the normal M3 addressing mode is re-established whenever the high-order register, mmrf, is loaded. (ie. written to).

3.2.4 24-BIT DMA IN M3 STANDARD (16-BIT) ADDRESSING MODE

The 512-ST provides M3 operation via the standard 16-bit bus addresses as specified by IEEE/696. In addition, in order to accommodate some non-standard variations, the 512-ST permits a hybrid operation of **standard** 16-bit (and thus M3) addressing by the CPU and **extended** addressing by DMA devices.

In either case, jumper J2-C must be installed "right" to enable standard 16-bit M3 addressing from the CPU. Jumper J2-B in the "left" position enables that same 16-bit addressing for DMA. In the "right" position, J2-B enables 24-bit DMA operation while enabling 16-bit M3 addressing for the CPU.

Jumper	Loc'n	Address Lines	Installed Left	Installed Right	Description & Comments
J4-D	K1	A7	A7=1	A7=0	Memory mapping
J3-C		A6	A6=1	A6=0	registers' most
J3-A		A5	A5=1	A5=0	significant nibble
J3-B		A4	A4=1	A4=0	of I/O address. (least significant nibble = reg #)
J3-A	H1	A23	OFS23=1	OFS23=0	Board addr. offset
J3-D		A22	OFS22=1	OFS22=0	Defines the origin
J3-C		A21	OFS21=1	OFS21=0	of the board in
J3-B		A20	OFS20=1	OFS20=0	the 16 Megabyte
J2-D		A19	OFS19=1	OFS19=0	physical
J2-F		A18	OFS18=1	OFS18=0	memory space.
J2-E		A17	OFS17=1	OFS17=0	(see Table 2.2)
J5-D	K6	PASS*	disabled	enabled	Pass (power-up/reset) mode select

Table 3.1 Addressing Jumpers
Standard (16-bit) M3 Addressing

Jumper	Loc'n	Installed Position	Description & Comments
J2-C	G1	(Left	Extended 24-bit Addressing)
		Right	Standard 16-bit (M3) non-DMA Addressing.
J2-B	G1	Left	16-bit (M3) DMA Addressing.
		Right	Extended 24-bit DMA Addressing and 16-bit (M3) CPU Addressing

Table 3.2 Address Mode Selection Jumpers
Standard Addressing

M3 MEMORY MANAGEMENT EXAMPLES

3.3.1 SAMPLE INITIALIZATION ROUTINE

The code shown below can be used as a simple guideline for loading the map values in a typical 20-bit initialization sequence. The following parameters will be used for the hypothetical S-100 system:

a. 8080 cpu
b. I/O base port = 80h
c. one 512-ST addressed at level zero - (00000-1ffffh)
d. registers mapped to the lowermost 64k (identical to pass mode addressing).

```
                ;
                ; Sample Initialize Routine:
                ;
0100                    ORG     100H

0080 =          MMR:    EQU     80H     ;I/O base address

0100 AF         INIT:   XRA     A       ;pick up a zero
0101 210501             LXI     H,IN1+1 ;set up pointer
0104 D380       IN1:    OUT     MMR     ;load map register
0106 34                 INR     M       ;next port
0107 3C                 INR     A       ;next register
0108 FE10               CPI     16      ;done?
010A C8                 RZ
010B C30401             JMP     IN1     ;no, continue
010E                    END
```

The execution of a routine of this type will effect the switch from pass mode to map mode after mmrf has been loaded. The memory address mapping will be as shown in Figures 3.1 and 3.3, mapped precisely to the same physical address space as the previous pass mode addressing.

3.3.2 SAMPLE BANK SWITCH ROUTINE

The following code switches three banks to the following physical bank numbers:

1. mmr9 to 19H 19000-19FFFH (100K-104K)
2. mmra to 1AH 1A000-1AFFFH (104K-108K)
3. mmrb to 1BH 1B000-1BFFFH (108K-112K)

```
                ;
                ; Sample Routine to Switch Three 4k Banks:
                ;
                ; mmr9-->19H, mmra-->1AH, mmrb-->1BH
                ;

0100            ORG     100H

0080 =          MMR:    EQU     80H     ;I/O base address

0100 3E19       SWITCH: MVI     A,19H   ;get starting bank number
0102 210A01             LXI     H,SW1+1 ;set up port pointer
0105 0E03               MVI     C,3     ;bank counter
0107 3689               MVI     M,MMR+9 ;establish port address
0109 D389       SW1:    OUT     MMR+9   ;load map register
010B 3C                 INR     A       ;next bank
010C 34                 INR     M       ;next map register
010D 0D                 DCR     C       ;done?
010E C8                 RZ
010F C30901             JMP     SW1     ;no, continue
0112                    END
```

The execution of the above routine will alter the memory map as shown in Figure 3.2. Note that any logical address in the range of 9000-BFFFH will now access 19000-1BFFFH until the map registers mmr9-mmrb are reloaded with new values.

3.3.3 SAMPLE TABLE DRIVEN BANK SWITCH ROUTINE

In some simple mapped addressing applications, a set of tables may suffice for switching banks. The following example shows a single 12-entry table for a 48k bank switch. A few more tables and a means to switch the table pointer might make a simple routine like this quite adequate for a multi-user I/O system if the memory size is small. Just be careful not to expect a routine like this one to initialize the system, because it won't. Registers mmr0 through mmrb are loaded by this routine but registers mmrc through mmrf are not. Register mmrf must be loaded in order to turn on map mode addressing.

The unlikely map table in this program and in the example on Figure 3.4 is shown mainly to illustrate that table entries need not follow a sequence, nor any particular pattern. The only restriction is that if memory is to be accessed, an existing board must reside in the address space requested by the mmr.

If it is necessary to leave a "hole" in the 64K logical address space, any number of the 16 4k increments of logical address can be "switched off" if 31 or less 512-ST's are installed in the system (less than 16 megabytes). Simply write an address belonging to the missing board(s) into each of the mmr's you wish to eliminate from the address map. The same value can be used in all the "switched off" mmr's, since no memory will be addressed by them. Use the blocks normally addressed by these mmr's in a "junkbox" of table entries in another user block somewhere.

```
                ; Sample Table Driven Map Register Load Routine:

0100                    ORG     100H

0080 =          MMR:    EQU     80H     ;I/O base address

0100 111401     LOAD:   LXI     D,MTAB  ;point to table base
0103 210C01             LXI     H,LD2+1 ;point to mmr port
0106 0E0C               MVI     C,12    ;load 12 registers
0108 3680               MVI     M,MMR   ;set up port address
010A 1A         LD1:    LDAX    D       ;get table entry
010B D380       LD2:    OUT     MMR     ;load map register
010D 34                 INR     M       ;next register
010E 13                 INX     D       ;next table entry
010F 0D                 DCR     C       ;done?
0010 C8                 RZ
0111 C30A01             JMP     LD1     ;no, continue

                  Map Load Table:

0114 0001124334MTAB:    DB      00H,01H,12H,43H,34H,45H ;0000-5FFFH
011A 565F4F3F2F         DB      56H,5FH,4FH,3FH,2FH,1FH ;6000-BFFFH
0120                    END
```

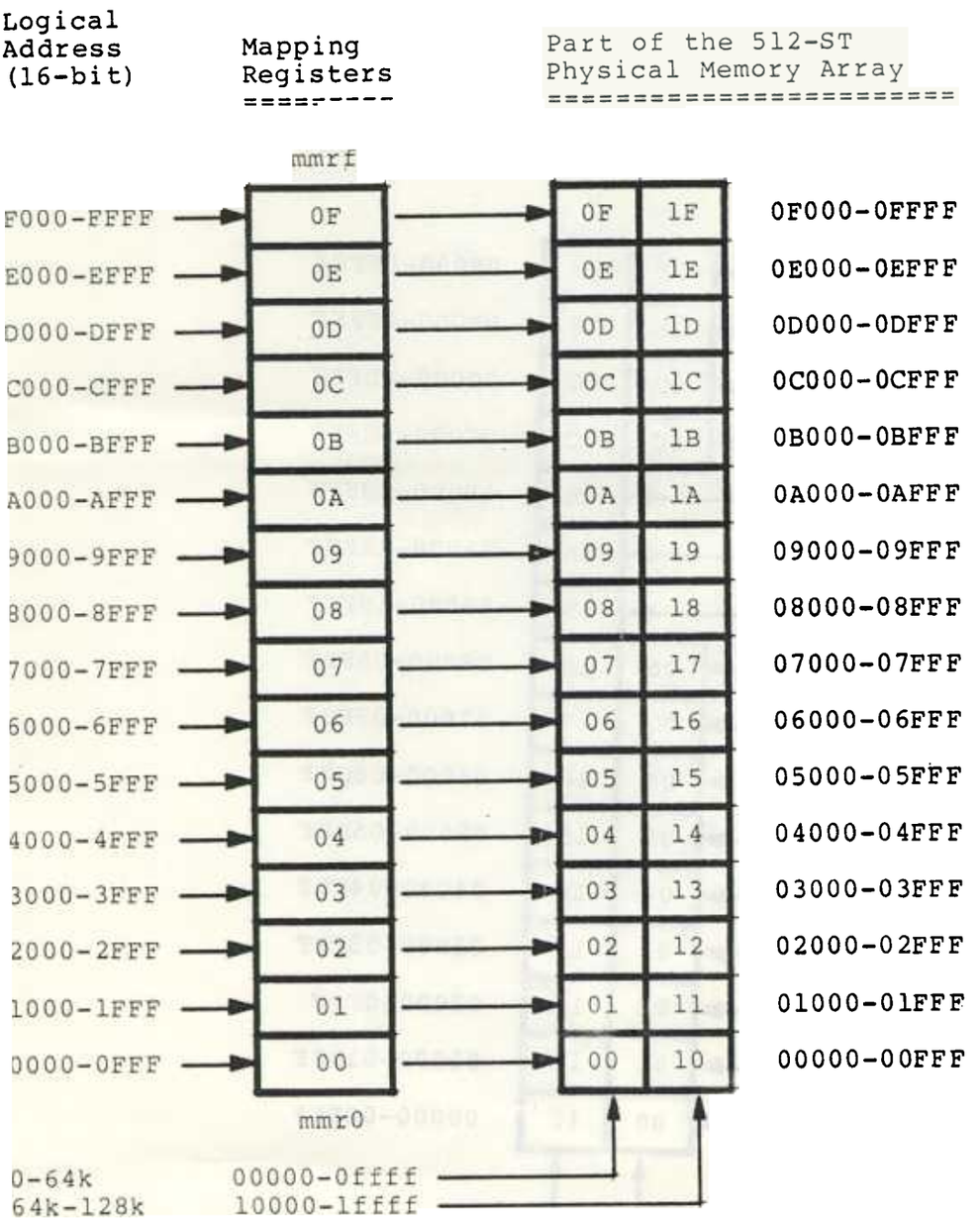


FIGURE 3.1 EXAMPLE 1
M3 MEMORY MAPPED ADDRESSING

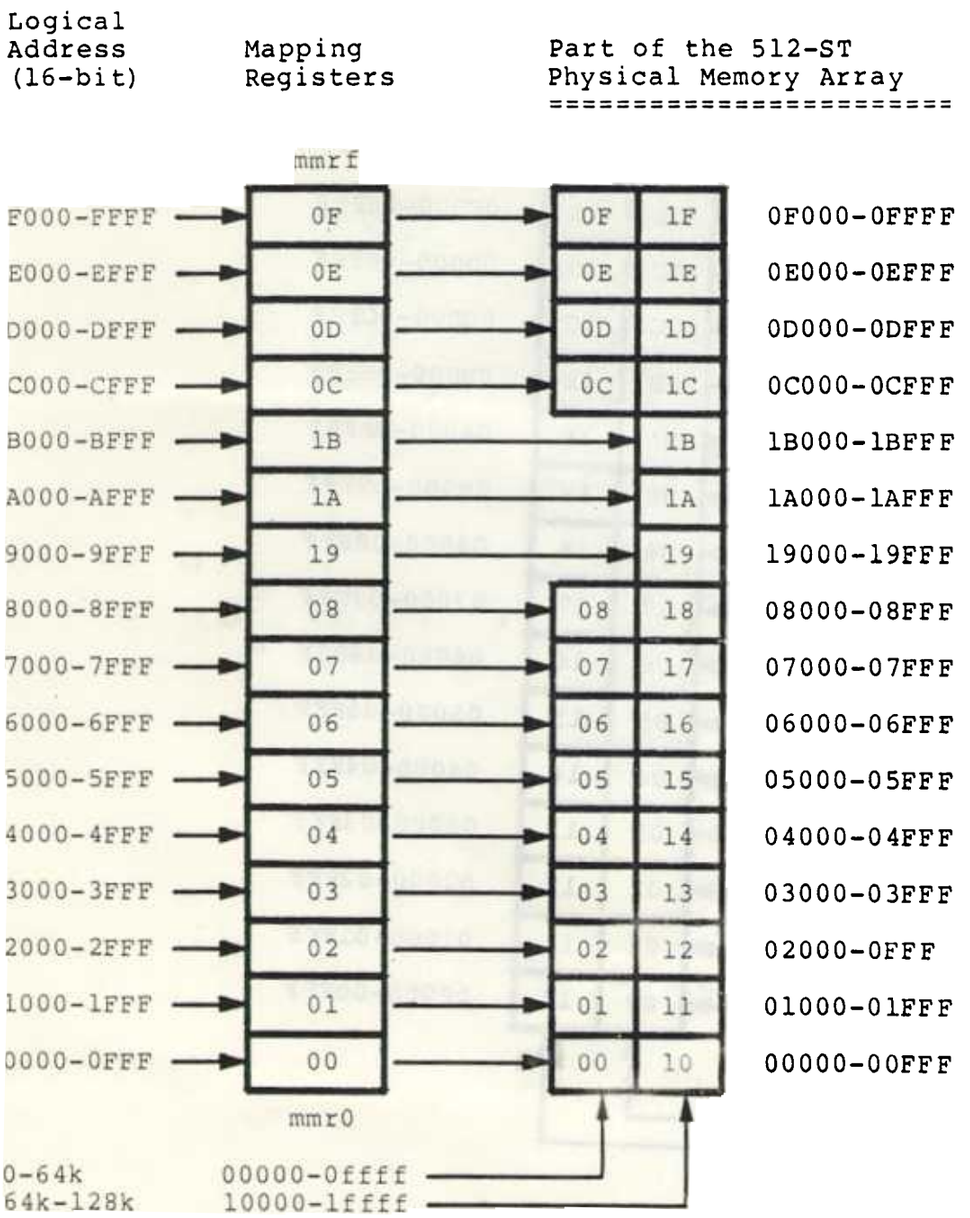


FIGURE 3.2 EXAMPLE 2
M3 MEMORY MAPPED ADDRESSING

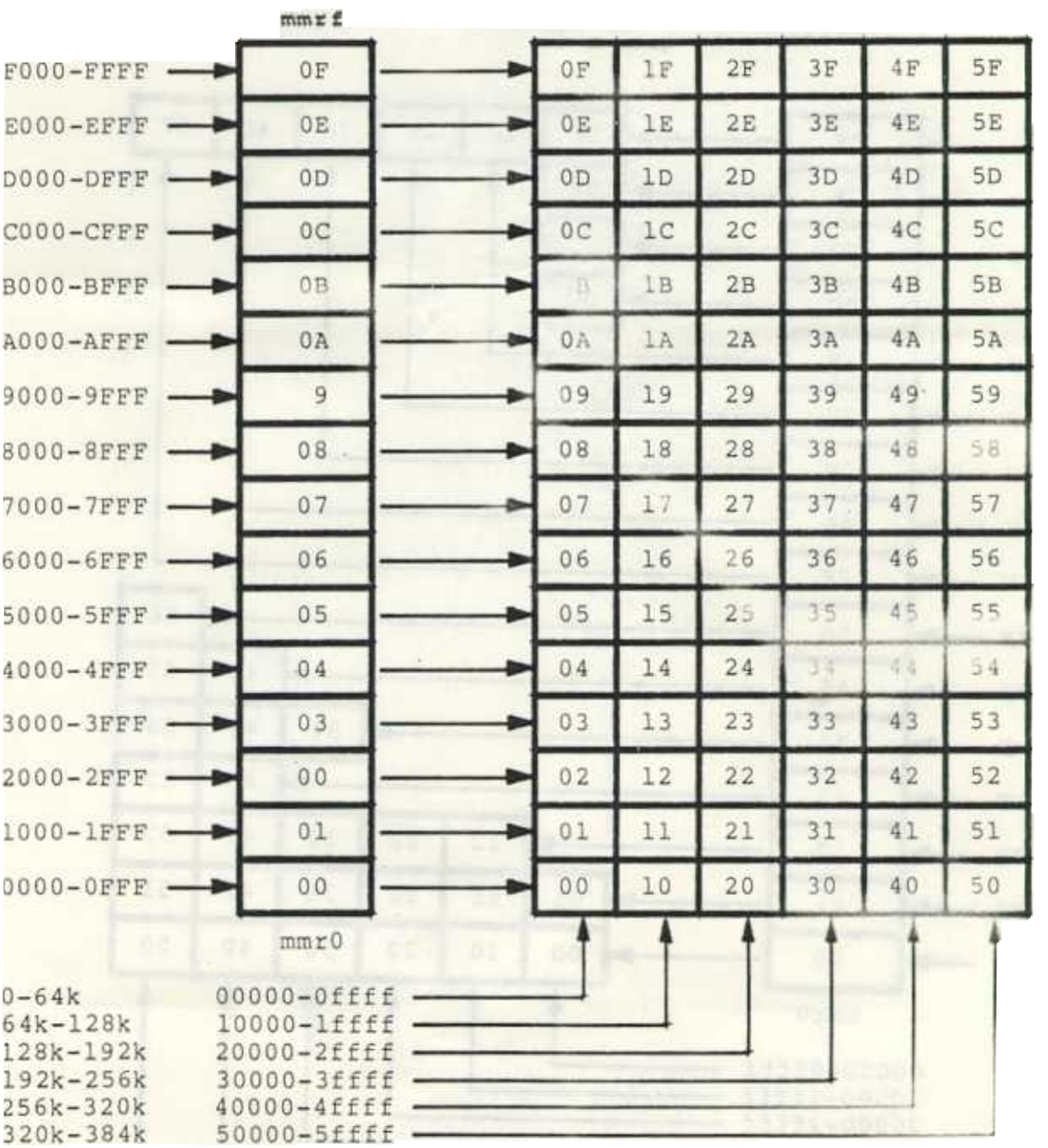


FIGURE 3.3 EXAMPLE 3
M3 MEMORY MAPPED ADDRESSING

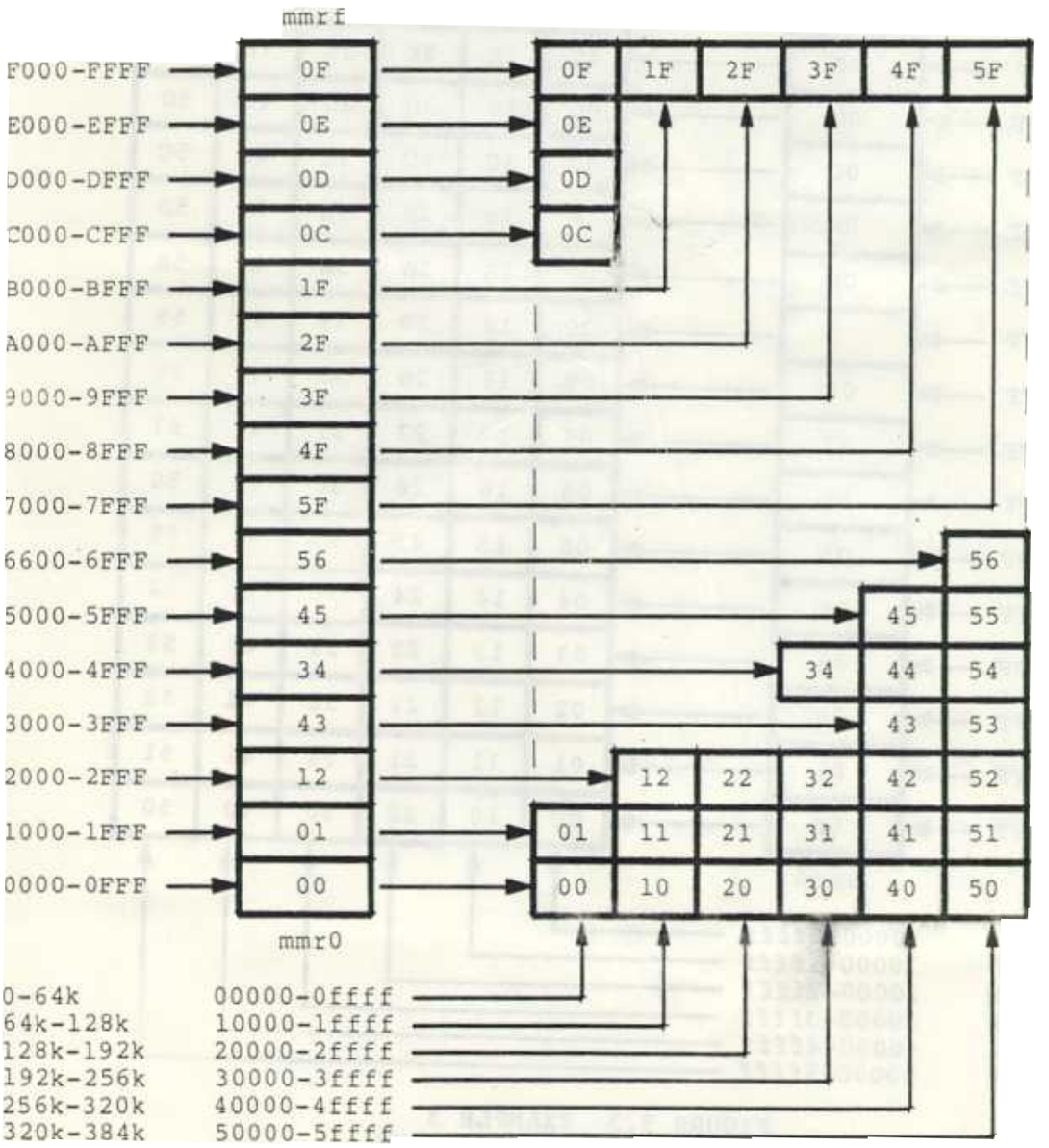


FIGURE 3.4 EXAMPLE 4
M3 MEMORY MAPPED ADDRESSING

SPECIAL FEATURES

BATTERY BACKUP

The 512-ST uses low power CMOS RAM memory chips, plus a separate power plane on the printed circuit board for those chips, to permit independent application of power from a backup battery source in case of failure of normal system power.

Bus pin 21 is listed in IEEE/696 as "undefined". In Macrotech systems, this bus line carries backup-battery power to CMOS RAM memory boards. Pin 21 is the board's battery power source when jumper J1A at location M2 is installed. If J1A is omitted or set left, the board will function normally, but data will not be retained in case of power failure. If J1A is set right, the contents of memory will be retained as long as the voltage on pin 21 remains between +2.3 and +4.0 volts.

The battery backup mode is invoked if PWRFAIL* (pin 13) is held low by the system powerfail logic. The 512-ST then disables its write enable and chip select logic and blocks all spurious memory accesses until PWRFAIL* returns false, indicating that normal power has been restored. The 512-ST will be in low-power standby mode while PWRFAIL* is asserted. This mode is particularly useful for Virtual Disk applications, since it assures the continued integrity of the contents of the Virtual Disk after either loss of power or a normal system shutdown.

To use the 512-ST's battery backup mode successfully, your system must have a backup power source (battery) capable of providing at least 80 milliamps of DC power with at least 2.4 volts to the board for the entire backup period. This high a current capability is needed because the CMOS RAM devices on the 512-ST are selected for speed rather than for low backup current requirement. Your board will probably draw considerably less.

Your system must also have a system power monitor circuit for at least the +8 volt supply, to drive the PWRFAIL* bus line. The best system power monitor is one that also senses the AC power to the computer power supply, to provide the earliest possible warning of impending power failure.

If bus pin 21 is already used by other boards in your system for some other purpose, you will have to use one of the other NDEF lines [65,66] for the Vbat battery backup line. J1A must be disconnected. Its center pin must be patched to the chosen NDEF bus pin.

4.3 EASY FIXES TO COMMON IEEE/696 DEVIATIONS

4.3.1 FLOATING LINES.

Certain older systems had no provision for some of the lines defined in IEEE/696 and used by the 512-ST. Whether or not they are driven, these lines must be pulled up high with resistors for the 512-ST to work reliably.

The 512-ST provides pullup resistors, jumper-selectable, for:

Bus pin 13	PWRFAIL*	J1C	set right
Bus pin 58	SXTRQ*	J5C	set right
Bus pin 67	PHANTOM*	J5A	set right (only needed if PHANTOM* is enabled by setting J5B left)

In some user systems, the bus terminator network has pullups to pull these lines high, even if no board in the system will drive them low. In other systems, more than one board may provide pullups for these lines (more than one Macrotech board, for instance). No more than one pullup should be enabled for each of these lines, so their open-collector drivers won't have to sink excess current.
If there is any doubt about this, however, it is best to use the onboard pullups, to insure that bus noise on these lines can't cause erratic behavior. Better safe than sorry.

4.3.2 POWER-OK IN ALPHA SYSTEMS

ALPHA MICRO 100L: The PWRFAIL* signal at bus pin 13 is reversed in function... it goes low, not high, when system power is okay. The AM100L is <u>not</u> listed as IEEE/696, so this is not illegal, but this will lock up the board's RAM array during system operation until fixed.
If backup capability is not needed, lift the right-hand end of R1 and tack it to either end of R3. This permanently enables the RAM array. Disconnect the pullup R3 from the bus signal by setting J1C left.
If backup capability is needed, a circuit patch is needed, an inverting stage. Break etch between bus pin 13 and jumper J1C/resistor R1; patch bus pin 13 to F2:1; patch jumper J1C/resistor R1 to F2:2. This patches a 74F04 inverter into the line. Disable the pullup R3 by setting J1C left.

JUMPER	LEFT		RIGHT
J1-A	-		pin 21 to battery plane
J1-B	-		pin 53 to GND
J1-C	-		PWRFAIL* pullup resistor
J2-A	20-bit M3		24-bit M3 addressing
J2-B	24-bit DMA		20-bit DMA (M3 only)
J2-C	24-bit ADDR		16-bit (M3) addressing
J2-D	OFS19 = 1	MEMORY ADDRESS SELECT [see table]	OFS19 = 0
J2-E	OFS17 = 1		OFS17 = 0
J2-F	OFS18 = 1		OFS18 = 0
J3-A	OFS23 = 1		OFS23 = 0
J3-B	OFS20 = 1		OFS20 = 0
J3-C	OFS21 = 1		OFS21 = 0
J3-D	OFS22 = 1		OFS22 = 0
J4-A	MMRA4 = 1	I/O ADDRESS SELECT [M3 mode only	MMRA4 = 0
J4-B	MMRA5 = 1		MMRA5 = 0
J4-C	MMRA6 = 1		MMRA6 = 0
J4-D	MMRA7 = 1		MMRA7 = 0
J5-A	-		PHANTOM* pullup
J5-B	PHANTOM* active		-
J5-C	-		SXTRQ* pullup
J5-D	Pass Mode active		

Table 5.1 Jumper Function Summary

Note: The following two tables are quick summaries of Tables 2.2.1 - 2.2.4. They provide jumper settings for the most commonly-used base addresses, labelled in commonly-used (inaccurate) decimal boundaries, such that "1,128K" means 1 Megabyte plus 128 Kilobytes. The hexadecimal addresses are accurate in both sets of tables, and should be used for cross-reference.

512-ST Board Base Address		-------- OFFSET: OFS23 - OFS17 ----------						
DECIMAL	HEX	ofs23 J3A	ofs22 J3D	ofs21 J3C	ofs20 J3B	ofs19 J2D	ofs18 J2F	ofs17 J2E
0K	000000	R	R	R	R	R	R	R
128K	020000	L	L	L	L	L	L	L
256K	040000	L	L	L	L	L	L	R
384K	060000	L	L	L	L	L	R	L
512K	080000	L	L	L	L	L	R	R
640K	0A0000	L	L	L	L	R	L	L
768K	0C0000	L	L	L	L	R	L	R
896K	0E0000	L	L	L	L	R	R	L
1M	100000	L	L	L	L	R	R	R
1,128K	120000	L	L	L	R	L	L	L
1,256K	140000	L	L	L	R	L	L	R
1,384K	160000	L	L	L	R	L	R	L
1,512K	180000	L	L	L	R	L	R	R
1,640K	1A0000	L	L	L	R	R	L	L
1,768K	1C0000	L	L	L	R	R	L	R
1,896K	1E0000	L	L	L	R	R	R	L
2M	200000	L	L	L	R	R	R	R
2,128K	220000	L	L	R	L	L	L	L
2,256K	240000	L	L	R	L	L	L	R
2,384K	260000	L	L	R	L	L	R	L
2,512K	280000	L	L	R	L	L	R	R
2,640K	2A0000	L	L	R	L	R	L	L
2,768K	2C0000	L	L	R	L	R	L	R
2,896K	2E0000	L	L	R	L	R	R	L
3M	300000	L	L	R	L	R	R	R

Table 5.2 - Board Address Selection

Note: "L" indicates jumper installed toward left of board
"R" indicates jumper installed toward right (away from regulator)

512-ST Board Base Address		-------- OFFSET: OFS23 - OFS17 ----------						
DECIMAL	HEX	ofs23 J3A	ofs22 J3D	ofs21 J3C	ofs20 J3B	ofs19 J2D	ofs18 J2F	ofs17 J2E
4M	400000	L	L	R	R	R	R	R
5M	500000	L	R	L	L	R	R	R
6M	600000	L	R	L	R	R	R	R
7M	700000	L	R	R	L	R	R	R
8M	800000	L	R	R	R	R	R	R
9M	900000	R	L	L	L	R	R	R
10M	A00000	R	L	L	R	R	R	R
11M	B00000	R	L	R	L	R	R	R
12M	C00000	R	L	R	R	R	R	R
13M	D00000	R	R	L	L	R	R	R
14M	E00000	R	R	L	R	R	R	R
15M	F00000	R	R	R	L	R	R	R
15,128K	F20000	R	R	R	L	L	L	L
15,256K	F40000	R	R	R	L	L	L	R
15,384K	F60000	R	R	R	L	L	R	L
15,512K	F80000	R	R	R	L	L	R	R
15,640K	FA0000	R	R	R	L	R	L	L
15,768K	FC0000	R	R	R	L	R	L	R

Table 5.3 - Board Address Selection

Note: "L" indicates jumper installed toward left of board
"R" indicates jumper installed toward right (away from regulator)