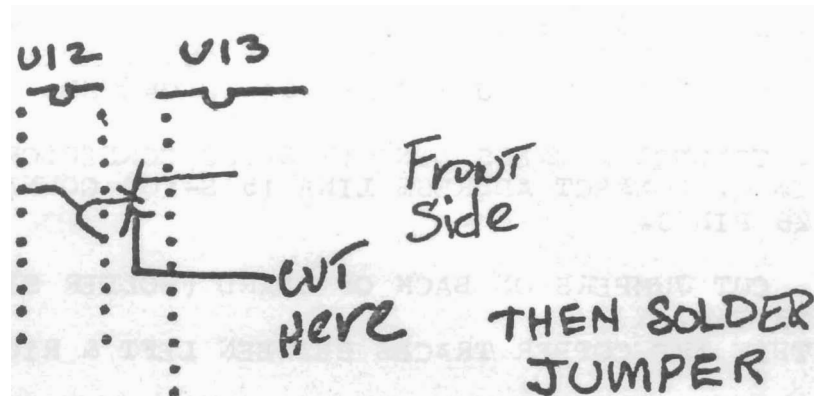
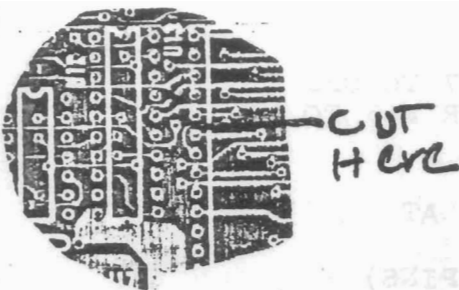


CONVERSION OF THE ITHICA INTERSYSTEMS IA-2030
 64K DYNAMIC RAM MEMORY BOARD TO 256K WHILE
 RETAINING ALL ITS FEATURES.

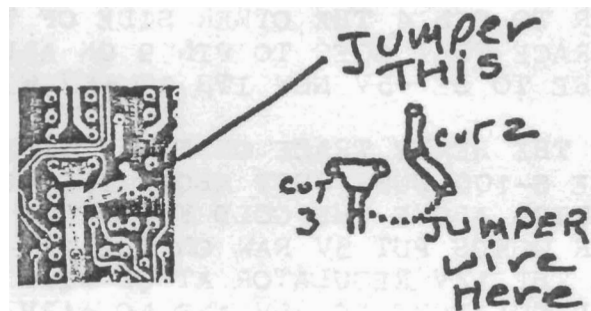
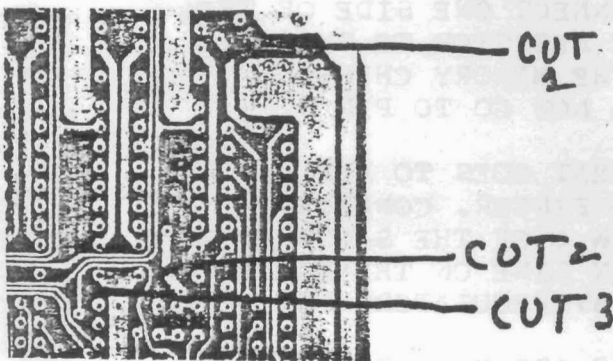
[WORD AND BYTE WIDE DATA TRANSFERS ON THE S-100 BUSS]

1. IF YOU HAVE A REV 'A' BOARD CAREFULLY CUT THE BELOW SHOWN TRACES. ON THE FRONT SIDE OF BOARD (COMPONENT SIDE) CUT THE TRACE BETWEEN PINS 16&17 OF U12 THEN SOLDER A JUMPER WIRE FROM U14 PIN 2 TO U9 PIN 11. THIS IS REQUIRED OF ALL REV 'A' BOARDS REGARDLESS OF THE 256K MODIFICATION OR NOT.

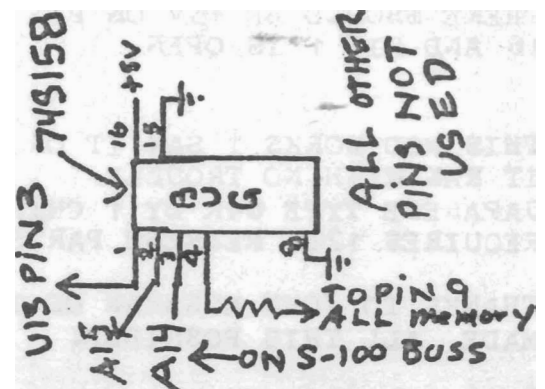
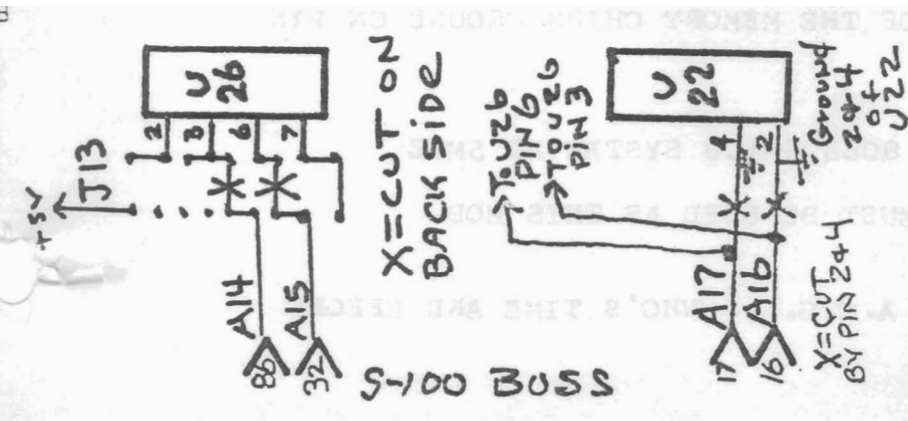
MAKE THESE CHANGES



2. ON REV 'A' BOARDS MAKE THE FOLLOWING CHANGES TO BRING BOARD UP TO 256K OF RAM.



3. THESE ARE THE CHANGES NECESSARY TO UP DATE THE ADDRESSING ALLOWING FOUR 64K BLOCKS THIS IS FOR THE FIRST 256K PAGE ADDRESSING ABOVE THIS REQUIRES USING THE NEXT HIGHER ADDRESS LINES.



3. DO NOT INSTALL ANY OF THE BYPASS CAPACITORS THAT ARE LOCATED ON THE THIRD ROW FROM THE TOP JUST BELOW THE SECOND ROW OF MEMORY CHIPS. DO NOT INSTALL CAPACITOR LABELED C6 ON RIGHT SIDE OF BOARD. DO NOT INSTALL CAPACITOR LABELED C1 ON UPPER LEFT SIDE OF BOARD. DO NOT INSTALL Q1 THE -5V REGULATOR LOCATED ON THE UPPER LEFT HAND SIDE OF BOARD.

4. ACQUIRE A 74S158 TYPE MUX AND GLUE IT TO BOARD FRONT SIDE DEAD BUG STYLE (LEGS UP) AT LOCATION TO THE RIGHT OF C25.

ABOVE U16 & U17 WITH PIN 1 TO THE LEFT SIDE OF BOARD.

5. U22 CONTROLS WHICH 256K BLOCK WITHIN THE 1 MEGABYTE SPACE. FOR THE FIRST 0 TO 256K CUT TRACES AT U22 PINS 2&4 AND TIE U22 PINS 2&4 TO GROUND.

6. CONNECT ADDRESS LINE 17 S-100 CONNECTOR #17 TO U26 PIN 6. CONNECT ADDRESS LINE 16 S-100 CONNECTOR #16 TO U26 PIN 3.

7. CUT JUMPERS ON BACK OF BOARD (SOLDER SIDE) AT J13 E&G.
(THEY ARE COPPER TRACES BETWEEN LEFT & RIGHT PINS)

8. FIND +5V ON BOARD AND CONNECT TO PIN 16 OF 74S158 (THE DEAD BUG!) FIND GROUND AND CONNECT TO PIN 8 OF THE 74S138. REMEMBER ITS UP SIDE DOWN SO GET THE PIN NUMBERS RIGHT.

9. CONNECT PIN 4 OF THE 74S158 TO A 30 OHM RESISTOR AND THEN TO PIN NUMBER 9 OF ALL THE MEMORY CHIPS CONNECT ONE SIDE OF THE RESISTOR TO PIN 4 THE OTHER SIDE OF THE RESISTOR TO THE HEAVY TRACE THAT GOES TO PIN 9 ON ALL THE MEMORY CHIPS. PIN 9 USE TO BE +5V NOW ITS A9 +5V WILL NOW GO TO PIN 8.

10. CUT THE HEAVY TRACE ON FRONT SIDE THAT GOES TO PIN 2 ON THE S-100 BUSS JUST ABOVE THE GOLD FINGER. CONNECT THE PORTION ABOVE THE GOLD FINGER TO PIN 1 OF THE S-100 BUSS IN OTHER WORDS PUT 5V RAW ON THE 12V RAW LINE ON THE BOARD REPLACE THE 12V REGULATOR AT Q2 WITH A 5V REGULATOR. NOW WE HAVE TWO 5V REGULATORS NC -5V AND NO +12V.

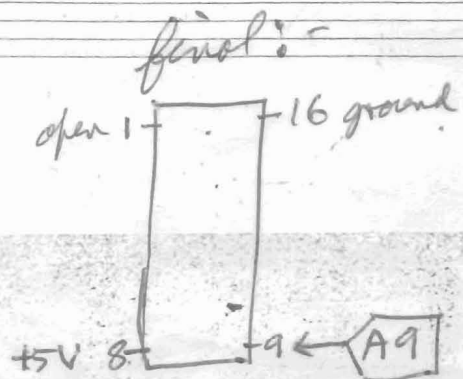
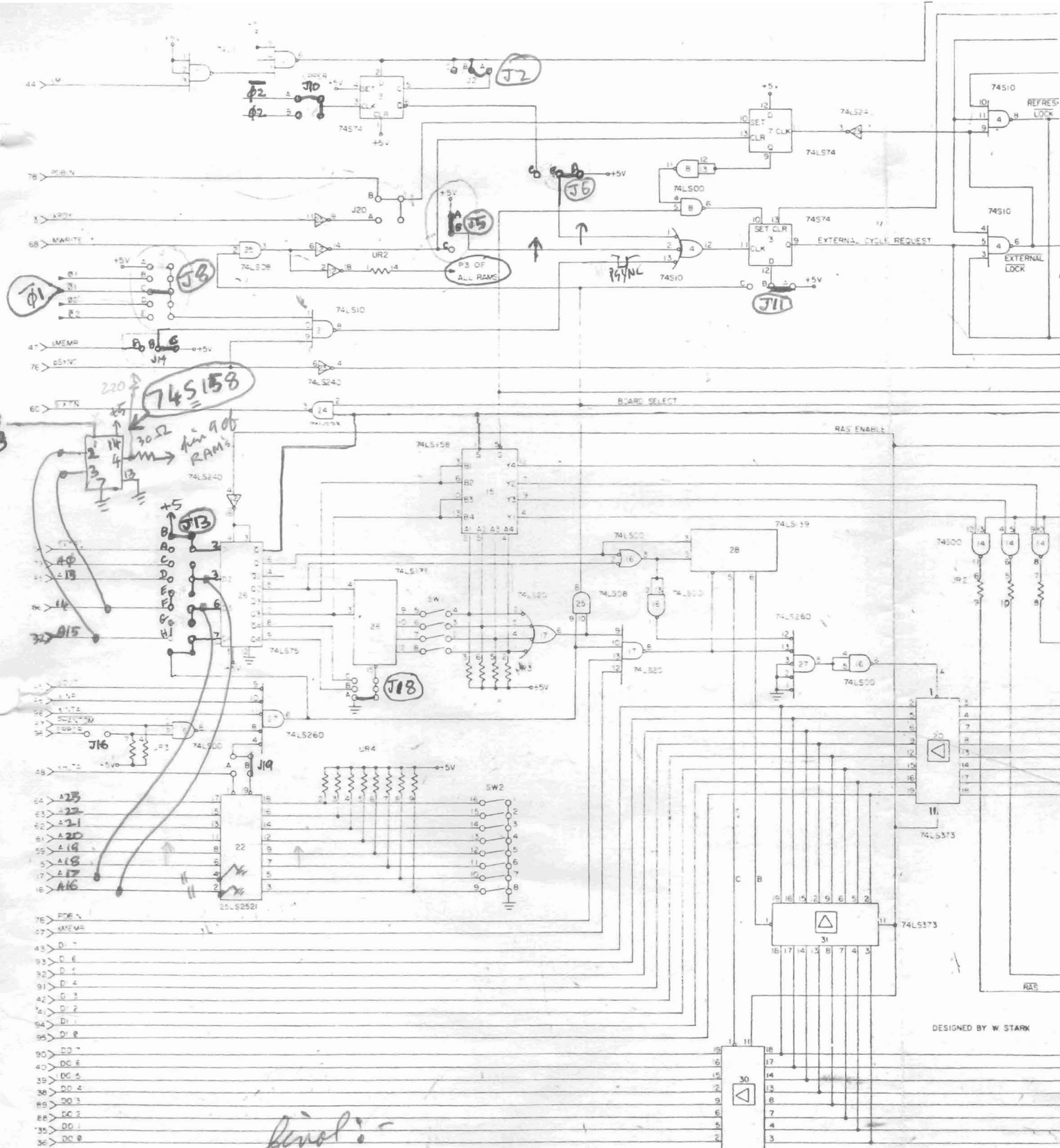
11. CONNECT PIN 2 OF THE 74S158 TO A15 S-100 BUSS PIN 32 AND CONNECT PIN 3 OF THE 74S158 TO A14 S-100 BUSS PIN 86. CONNECT PIN 15 OF THE 74S158 TO GROUND.

12. THIS SHOULD DO IT. CHECK ALL VOLTAGES WITH OUT THE CHIPS INSERTED THERE SHOULD BE +5V ON PIN 8 OF THE MEMORY CHIPS GROUND ON PIN 16 AND PIN 1 IS OPEN.

THIS MOD WORKS I SAW IT ON AN 8088 S-100 SYSTEM AT 5MHZ IT RAN WITH NO TROUBLE.

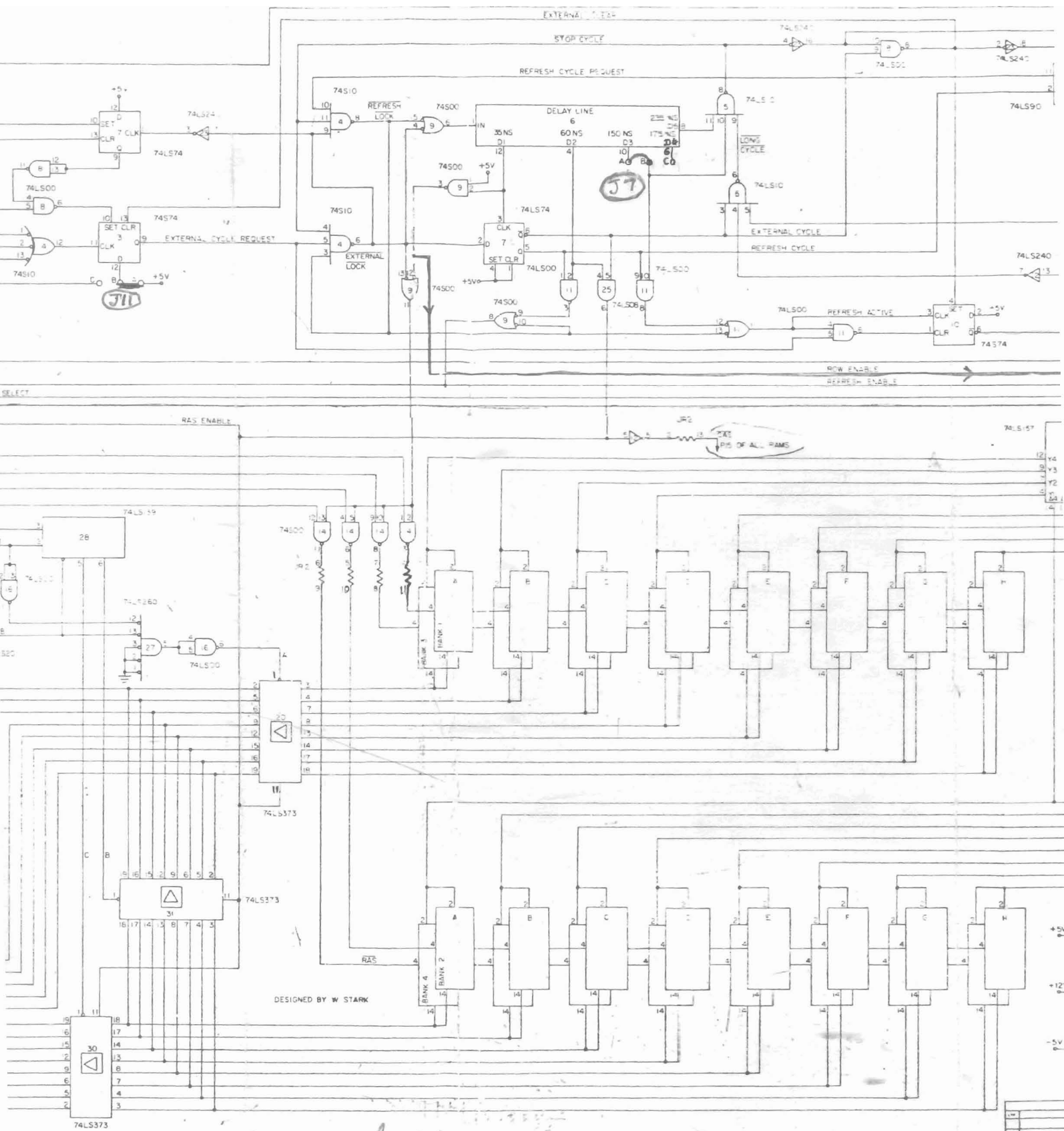
JAPANESE TYPE 64K BY 1 CHIPS MUST BE USED AS THIS MOD REQUIRES 128K REFRESH PARTS.

THANKS TO JOHN MONAHAN OF THE A.C.G.N.J. WHO'S TIME AND EFFORT MADE ALL THIS POSSIBLE.



check these
voltage
before putting
in 64K ram
chips.

Delay line from
Engineered
Components Co
DM-10-43
EC² 30

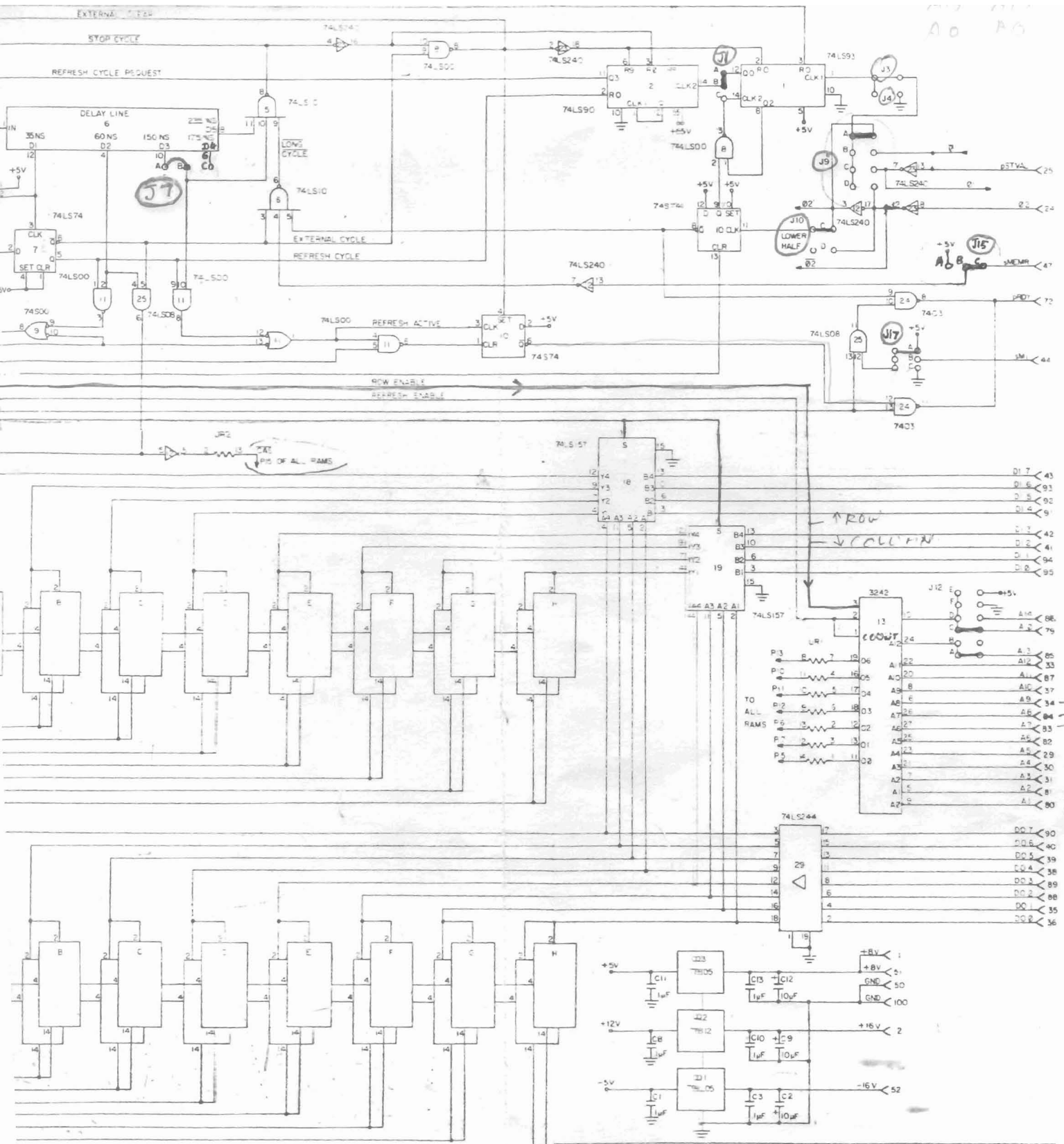


Delay line from
 Engineered
 Components Co.
 DM-10-433

jumpers are for 0-256K with
 5MHz 2808 (IAD) board
 5MHz 8088 (ACOM) board

EC² 3082

low
 setting
 K RAM



confers one for 0-256K with
 5MHz 280B (IAI) board
 5MHz 8098 (ACOM) board

J. MONAHAN

REV	DESCRIPTION	DATE	APPROVED	SCALE	SHEET	OF
1						
2						
3						
4						
5						
6						
7						
8						
9						
10						

InterSystems
 IYBACA, NEW YORK 10008
 UNLESS OTHERWISE NOTED
 64K DYNAMIC REV A
 DATE: 11/15/79
 NUMBER: A 2050