
OWNER'S MANUAL

Model 2710

4-Port Serial I / O Interface



California Computer Systems

CCS MODEL 2710

4-PORT SERIAL INTERFACE

OWNER'S MANUAL

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CHAPTER 1

INTRODUCTION

Each of the 2710's four serial ports features an 8250 Asynchronous Communications Element (ACE). This chip converts serial data received from a peripheral device or modem to parallel data, and parallel data transmitted by the processor to serial data. Data format options such as word length, parity, and number of stop bits are software-selectable. A number of operation and error status bits are maintained and can be read by the processor at any time. The chip also provides full handshaking control and a programmable, prioritized interrupt capability. In addition, each ACE includes a programmable baud rate generator which allows specification of the transmitter and receiver clock rates.

To the four ACEs CCS has added the circuitry necessary for a user-supplied 2716-type 2K EPROM, including FF Detect for byte-by-byte overlay. This allows convenient on-board storage of peripheral driver routines or patches. FF Detect circuitry disables output from the board whenever an unprogrammed location (all 1's, or FFh) is addressed, allowing other system memory at the same location to place data on the bus without conflict.

A number of features highlight CCS'S implementation of the ACEs and the EPROM. The base addresses are jumper-selectable, the EPROM to any 2K boundary within 64K, the serial ports to any multiple of 32 between 0 and 255. Jumpers also allow selection of either internal (ACE) or external (peripheral) generation of the ACE receiver clocks. An Interrupt Header provides additional flexibility, allowing connection of each ACE's interrupt output to the S-100 maskable interrupt line or to any one of the eight S-100 Vectored Interrupt pins.

FIGURE 1.1. 2710 BLOCK DIAGRAM

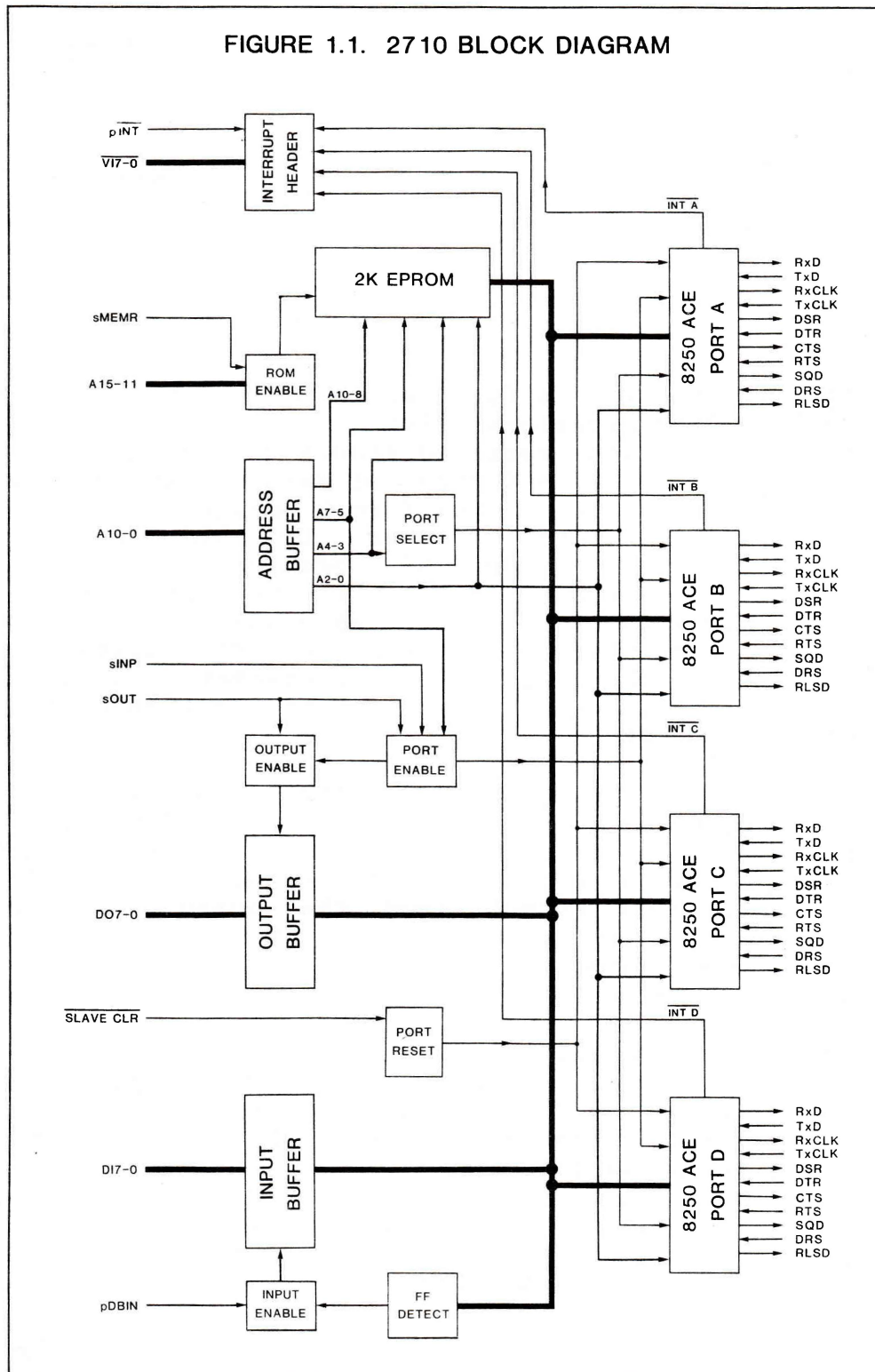
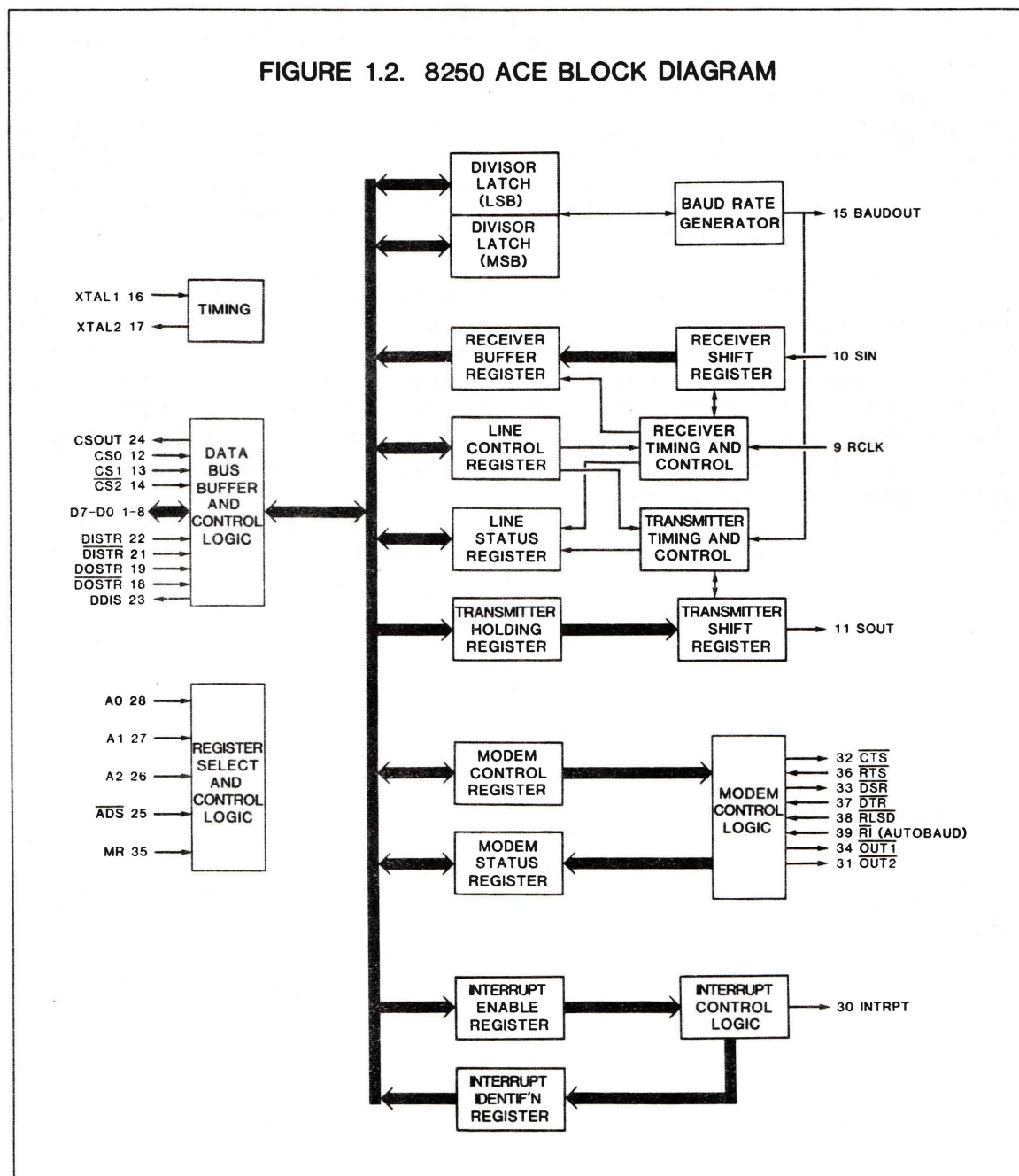


FIGURE 1.2. 8250 ACE BLOCK DIAGRAM



The 2710 has been designed for optimum system compatibility. As described above, port and memory base addresses are user-selectable, preventing address conflicts with fixed-address components of a system. The serial ports offer extensive format flexibility under software control. To further ensure compatibility with a wide range of peripherals, the port interfaces support configurations A through F of the RS-232-C specifications. Additionally, in order to place the least possible burden on a system's S-100 bus drivers, the 2710 has been designed to place no more than one TTL load on any S-100 bus line. Low-power Schottky and MOS devices used on the 2710 ensure that power consumption is minimal.

Throughout this manual, an asterisk following a signal name/mnemonic indicates a low-active signal (e.g., pINT*). Also, should you have occasion to refer to an 8250 data sheet, please note that the labels of 8250 pin pairs RTS*/CTS* and DTR*/DSR* in the data sheet are opposite to the labels in this manual. The labels have been reversed to make them consistent with the RS-232-C interface lines to which the pins connect.

CHAPTER 2

CONFIGURING THE 2710

2.1 JUMPERS

The 2710 includes several options which must be jumper-configured by the user. Figure 2.1 shows the locations of the jumpers on the board. To set a jumper, firmly seat a blue shorting plug over the two header pins corresponding to the desired setting.

2.1.1 PORT ADDR

The base address of the four serial ports is set on PORT ADDR jumpers 7-5; the jumper settings correspond to address bits A7-A5. Table 2.1 shows the jumper settings for all possible base addresses.

TABLE 2.1

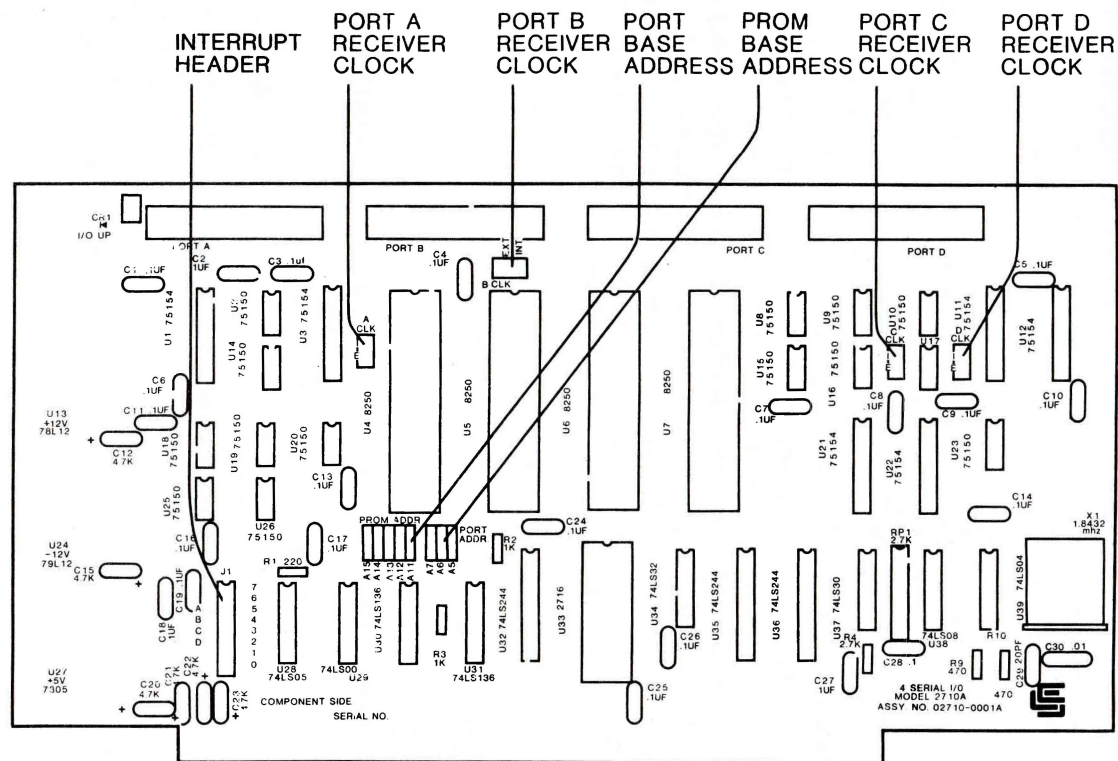
PORT BASE ADDRESSES

A7	A6	A5	HEX	DEC
0	0	0	00	0
0	0	1	20	16
0	1	0	40	32
0	1	1	60	48
1	0	0	80	64
1	0	1	A0	80
1	1	0	C0	96
1	1	1	E0	112

SET TO →

A0, A8, B0, B8
A B C D

FIGURE 2.1. 2710 JUMPER LOCATIONS



2.1.2 PROM ADDR

The five most significant bits of the base address of the on-board PROM are set on PROM ADDR jumpers 15-11. Thus the PROM may reside in any 2K block of system memory. Table 2.2 shows the jumper settings for any 2K block.

2.1.3 CLK A, B, C, D

Setting a CLK jumper to I (Internal) causes the corresponding port's Rx clock to be controlled by the port's Tx clock, as determined by that port's Divisor Latch. Setting a CLK jumper to E (External) causes the corresponding port's Rx clock to be controlled by RS-232-C line TxSET (DTE). The I position is topmost on jumpers A, C, and D, and rightmost on jumper B.

TABLE 2.2. ROM ADDRESSES

ADDRESS BITS					ROM ADDRESS	
A15	A14	A13	A12	A11	K=1024	HEX
0	0	0	0	0	0K	0000
0	0	0	0	1	2K	0800
0	0	0	1	0	4K	1000
0	0	0	1	1	6K	1800
0	0	1	0	0	8K	2000
0	0	1	0	1	10K	2800
0	0	1	1	0	12K	3000
0	0	1	1	1	14K	3800
0	1	0	0	0	16K	4000
0	1	0	0	1	18K	4800
0	1	0	1	0	20K	5000
0	1	0	1	1	22K	5800
0	1	1	0	0	24K	6000
0	1	1	0	1	26K	6800
0	1	1	1	0	28K	7000
0	1	1	1	1	30K	7800
1	0	0	0	0	32K	8000
1	0	0	0	1	34K	8800
1	0	0	1	0	36K	9000
1	0	0	1	1	38K	9800
1	0	1	0	0	40K	A000
1	0	1	0	1	42K	A800
1	0	1	1	0	44K	B000
1	0	1	1	1	46K	B800
1	1	0	0	0	48K	C000
1	1	0	0	1	50K	C800
1	1	0	1	0	52K	D000
1	1	0	1	1	54K	D800
1	1	1	0	0	56K	E000
1	1	1	0	1	58K	E800
1	1	1	1	0	60K	F000
1	1	1	1	1	62K	F800

2.2 THE INTERRUPT HEADER

The Interrupt Header allows the 2710 to operate in both polled and vectored interrupt environments. Each ACE's interrupt request line (header pins labeled A, B, C, and D) may be jumpered to any one of the eight S-100 Vectored Interrupt lines VI0-VI7* (pins labeled 0-7) or to pINT*.

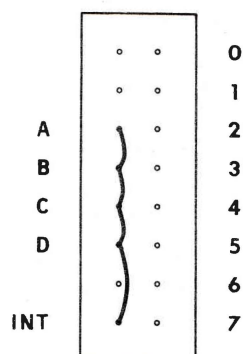
POLLED INTERRUPT
CONFIGURATION

FIGURE 2.2

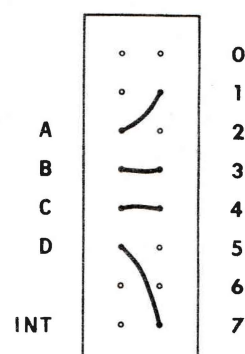
VECTORED INTERRUPT
CONFIGURATION

FIGURE 2.3

(pin labeled INT). Jumper wires are soldered to the header cover, which plugs into the header socket. Figure 2.2 illustrates the header configured for a polled interrupt environment. Figure 2.3 illustrates the header configured for a vectored environment, with Ports A, B, C, and D interrupting on VII*, VI3*, VI4* and VI7* respectively. For further discussion of polled and vectored interrupts, see Section 4.1.5.

2.3 CABLE CONSTRUCTION

Because peripherals compatible with the 2710 use a wide variety of connector configurations, no cables are included with the board and you will need to build or separately purchase the necessary cables. Cables to run from the 2710 serial ports to the back of the mainframe require a polarized female 26-pin connector (T&B/Ansley 609-2603 or AMP 88423-5) at the 2710 end and usually a female DB-25S connector at the other end. Two cables with these connectors are available separately from CCS: Product 7325A, which is 9 inches long, and Product 2000A, which is 18 inches.

The cables necessary to connect your peripherals to the mainframe connectors depend on the requirements of your peripherals. The manuals for your peripheral devices should provide the necessary information.

See Appendix A for pinouts of the 2710 serial port and RS-232-C interface connectors.

2.4 JUMPERING IN RESET*

If your system does not assert SLAVE CLR* (EXT CLR*) when RESET* is asserted, the 2710 will not be reset when the bus master (CPU) is reset. Cromemco-based systems, for example, will not automatically assert SLAVE CLR* whenever RESET* is asserted. To cause the 2710 to be reset with the bus master in such systems, cut the trace between pins 1 and 2 of U29 and jumper pin 2 to bus connector pin 75, RESET*.

This modification is unnecessary with CCS systems as well as with most other CPUs and motherboards on the market.

CHAPTER 3

PROGRAMMING INFORMATION

This chapter provides bit-by-bit descriptions of each ACE register as implemented on the 2710. Each ACE includes ten accessible registers. Table 3.1 shows the relative addresses of each port. Address bits A7-A5 select the board if they match the Port Address jumper settings, while bits A4 and A3 select one of the four ports. Address bits A2-A0 select the register. Table 3.2 gives the the formats and addresses of these registers. (A software register pointer and read only/write only register pairs allow more than eight registers in an eight-address block.)

[NOTE: The description of the 8250 registers in this manual is complete; the user should not need to consult an 8250 data sheet. Users who nevertheless consult a data sheet for whatever reason should be aware that some bits are uniquely implemented on the 2710. In all cases it should be assumed that if the data sheet and this manual differ, the information in this manual applies. Also, the labeling of the 8250 pin pairs CTS/RTS and DTR/DSR in this manual is the reverse of the labeling in an 8250 data sheet. This change has been made to reduce confusion by making the ACE pin labels consistent with the RS-232-C lines to which the pins are connected.]

TABLE 3.1. PORT SELECTION

INPUTS		ENABLED PORT	PORT ADDRESS	
A4	A3		HEX	BINARY
0	0	Port A	(Even X)0-7	XXX00000-XXX00111
0	1	Port B	(Even X)8-F	XXX01000-XXX01111
1	0	Port C	(X+1)0-7	XXX10000-XXX10111
1	1	Port D	(X+1)8-F	XXX11000-XXX11111

C = 10110110

TABLE 3.2a. 8250 ACCESSIBLE REGISTERS

BINARY ADDRESS		xxxx x000	xxxx x000	xxxx x000	xxxx x001	xxxx x001
HEX ADDRESS		X0/X8	X0/X8	X0/X8	X1/X9	X1/X9
DIVISOR LATCH BIT		0	0	1	1	0
OPERATION		Read Only	Write Only	Read/Write	Read/Write	Read/Write
REGISTER		Receiver Buffer Register	Transmitter Holding Register	Baud Rate Divisor Latch (LSB)	Baud Rate Divisor Latch (MSB)	Interrupt Enable Register
BIT	0	DI0	DO0	Bit0	Bit 8	Received Data Available
	1	DI1	DO1	Bit1	Bit 9	Transmitter Holding Register Empty
	2	DI2	DO2	Bit 2	Bit 10	Receiver Line Status
	3	DI3	DO3	Bit 3	Bit 11	Modem Status
	4	DI4	DO4	Bit 4	Bit 12	0
	5	DI5	DO5	Bit 5	Bit 13	0
	6	DI6	DO6	Bit 6	Bit 14	0
	7	DI7	DO7	Bit 7	Bit 15	0

EACH PORT
USES 6
CONSECUTIVE
ADDRESSES

A0-A5

A8-AD

B0-B5

B8-BD

TABLE 3.2b. 8250 ACCESSIBLE REGISTERS

xxxx x010	xxxx x011	xxxx x100	xxxx x101	xxxx x110	BINARY ADDRESS	
X2/XA	X3/XB	X4/XC	X5/XD	X6/XE	HEX ADDRESS	
X	X	X	X	X	DIVISOR LATCH BIT	
Read Only	Read/Write	Read/Write	Read/Write	Read/Write	OPERATION	
Interrupt Identification Register	Line Control Register	Modem Control Register	Line Status Register	Modem Status Register	REGISTER	
Interrupt Pending	Word Length Select 0	Data Set Ready	Data Ready	Delta RTS	0	BIT
Interrupt Identification Bit 0	Word Length Select 1	Clear To Send	Overrun Error	Delta DTR	1	
Interrupt Identification Bit 1	Stop Bit Select	Received Line Signal Detector	Parity Error	Trailing Edge TxD	2	
0	Parity Enable	Signal Quality Detector	Framing Error	Delta DRS	3	
0	Even Parity Select	Loop	Break Interrupt	Request To Send	4	
0	Stick Parity	0	Transmitter Holding Register Empty	Data Terminal Ready	5	
0	Set Break	0	Transmitter Shift Register Empty	Auto-Baud (TxD)	6	
0	Divisor Latch Access Bit	0	0	Data Rate Select	7	

MODEM STATUS

BASE + 5

BD + 05

= BD

0BDH

MODEM STATUS REGISTER

RTS Δ = 01

DTR = 20

3.1 LINE CONTROL REGISTER

Writing to this register allows the programmer to control the format of asynchronous data transfer. The register may also be read, allowing the programmer to inspect the data format and eliminating the need for storage of the register contents in system memory.

Bits 0-1

WORD LENGTH SELECT:
Length of the data character is determined by these two bits, as shown in Table 3.3.

WLS 1	WLS 0	WORD LENGTH
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

WORD LENGTH SELECTION
TABLE 3.3

Bit 2

STOP BIT SELECT: If this bit is a 0, one stop bit is generated or checked. If it is a 1, 2 stop bits are generated or checked, except with 5-bit words, in which case 1 stop bit is generated/checked.

Bit 3

PARITY ENABLE: If this bit is a 1, a parity bit is generated or checked. A 0 in this bit inhibits parity.

Bit 4

EVEN PARITY SELECT: When this bit is a 1 and parity is enabled, even parity is generated/checked. A 0 in this bit selects odd parity.

Bit 5

STICK PARITY SELECT: If parity is enabled and this bit is a 1, the same value will always be generated/checked in the parity bit position: a 0 if Bit 4 is 1, a 1 if Bit 4 is 0.

Bit 6

SET BREAK CONTROL: When this bit is a 1, the transmitted data (through SOUT onto RxD) is held at the 0 (spacing) state. Normal data transmission can occur only when this bit is cleared (0). The spacing signal can be used by the CPU to alert a terminal.

Bit 7 DIVISOR LATCH ACCESS: If this bit is a 1, the Least Significant Byte and the Most Significant Byte of the Divisor Latches are accessed when inputs A2-A0 are 000 and 001 respectively. When this bit is 0, either the Transmitter Holding Register (Write Only) or Receiver Buffer (Read Only) is addressed by 000 and the Interrupt Enable Register by 001.

3.2 TRANSMITTER HOLDING REGISTER

Parallel data is written to this write-only register for conversion to serial data and transmission to the peripheral via SOUT and RxD. When Bit 7 (Divisor Latch Access) of the Line Control Register and Address Bits A2-A0 are all 0 and pWR* is low, the character on the data bus will be latched into the Transmitter Holding Register.

3.3 RECEIVER BUFFER REGISTER

Serial data received from a peripheral and read according to the format determined by Line Control Register Bits 0-5 is converted to parallel data and latched into the Receiver Buffer. Data in this read-only register is gated onto the 2710 data bus when the Divisor Latch Access Bit and inputs A2-A0 are all 0.

3.4 DIVISOR LATCHES

These registers must be loaded with the appropriate baud rate divisor during initialization to ensure operation at the proper baud rate. For the low byte of the 16-bit divisor to be written or read, the Divisor Latch Access Bit must be 1 and A2-A0 must all be 0. Accessing the high byte requires the same conditions except that A0 is 1. Table 3.4 shows the divisors (in decimal, hexadecimal, and binary forms) for selected common baud rates.

TABLE 3.4. DIVISORS FOR COMMON BAUD RATES

BAUD RATE	DIVISOR			PCT. ERROR
	DEC	HEX	BINARY	
50	2304	0900	0000 1001 0000 0000	-
75	1536	0600	0000 0110 0000 0000	-
110	1047	0417	0000 0100 0001 0001	0.026
134.5	857	0359	0000 0011 0101 1001	0.058
150	768	0300	0000 0011 0000 0000	-
300	384	0180	0000 0001 1000 0000	-
600	192	00C0	0000 0000 1100 0000	-
1200	96	0060	0000 0000 0110 0000	-
1800	64	0040	0000 0000 0100 0000	-
2000	58	003A	0000 0000 0011 1010	0.69
2400	48	0030	0000 0000 0011 0000	-
3600	32	0020	0000 0000 0010 0000	-
4800	24	0018	0000 0000 0001 1000	-
7200	16	0010	0000 0000 0001 0000	-
9600	12	000C	0000 0000 0000 1110	-
19200	6	0006	0000 0000 0000 0110	-
38400	3	0003	0000 0000 0000 0011	-
56000	2	0002	0000 0000 0000 0010	2.86

Immediately after either Divisor Latch is loaded, the Baud Counter is loaded with the new value. This eliminates delays that might result from the Baud Counter having to finish the old count before the new count could be loaded.

3.5 LINE STATUS REGISTER

The first seven bits of this register provide status information regarding data transfer, as described below.

- Bit 0 DATA READY: This bit is set to 1 when an assembled character is available in the Receiver Buffer Register. A read of the Receiver Buffer register resets this bit; the bit may also be reset by writing a 0 directly into it.
- Bit 1 OVERRUN ERROR: A 1 in this bit indicates that a character in the Receiver Buffer Register was not read before the next character was transferred into the register. Reading the Line Status Register resets this bit.
- Bit 2 PARITY ERROR: A 1 in this bit indicates that the proper parity (depending on the state of the Even Parity Select bit) was not detected in the received data. (Parity will be checked only if the Parity Enable bit is set.) This bit is reset when the processor reads the Line Status Register.

- Bit 3 FRAMING ERROR: A 1 in this bit indicates that a received character lacked a valid Stop Bit--i.e., that the bit following the last data or parity bit was a 0. Reading the Line Status Register resets this bit.
- Bit 4 BREAK INTERRUPT: This bit is set to 1 when TxD is 0 for longer than the period between and including the start and stop bits.
- Bit 5 TRANSMITTER HOLDING REGISTER EMPTY: This bit is set to 1 when a character is transferred from the Transmitter Holding Register to the Transmitter Shift Register. It is reset to 0 when a new character is loaded into the Transmitter Holding Register.
- Bit 6 TRANSMITTER SHIFT REGISTER EMPTY: When this read-only bit is set to 1, the Transmitter Shift Register is idle.
- Bit 7 This bit is set permanently to 0.

3.6 INTERRUPT IDENTIFICATION REGISTER

The 8250 is capable of generating interrupts for any of four types of interrupt conditions. This three-bit read-only register, when addressed, indicates the type of the highest-priority interrupt pending. Table 3.5 shows the four types of interrupts, their priority levels and identification codes, and the operation necessary to reset the Interrupt Identification Register (IIR). After the IIR has been read, no other other interrupt conditions will be acknowledged until the interrupt indicated by the IIR has been serviced.

- Bit 0 INTERRUPT PENDING: This bit can be polled to determine whether an interrupt condition exists. A 0 indicates that an interrupt is pending.
- Bits 1-2 INTERRUPT IDENTIFICATION: When Bit 0 is 0, the type of the highest priority interrupt pending is encoded by these two bits, as indicated in Table 3.5.
- Bits 3-7 These five bits are always 0.

TABLE 3.5. INTERRUPT CONDITIONS

INTRPT ID BIT		PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT CONDITION	RESET CONDITION
Bit 1	Bit 0				
1	1	First	Receiver Line Status	OE, PE, FE or BI (Bits 1-4) Set	Read of Line Status Register
1	0	Second	Received Data Available	Data in Receiver Buffer	Read of Receiver Buffer
0	1	Third	Tx Holding Register Empty	Tx Holding Register Empty	Read of IIR or Read of TxHR
0	0	Fourth	Modem Status	Change in RTS, DTR, TxD, or DRS	Read of Modem Status Register

3.7 INTERRUPT ENABLE REGISTER

This four-bit register allows independent enabling or disabling of the four interrupt types identified in Table 3.5. If all interrupts are disabled, the INTRPT output of the 8250 and the Interrupt Identification Register are also disabled.

Bit 0 RECEIVED DATA AVAILABLE INTERRUPT: A 1 in this bit enables interrupts when Bit 0 of the Line Status Register is a 1.

Bit 1 TRANSMITTER HOLDING REGISTER EMPTY INTERRUPT: A 1 in this bit enables interrupts when Bit 5 of the Line Status Register is a 1.

Bit 2 RECEIVER LINE STATUS INTERRUPT: A 1 in this bit enables interrupts when a receiver error or break condition exists (i.e., when one of Bits 1-4 of the Line Status Register is a 1).

Bit 3 MODEM STATUS INTERRUPT: A 1 in this bit enables interrupts when one of interface lines RTS, DTR, or RLSD changes state, or when a high-to-low transition occurs at AUTOBAUD (TxD). Because high-to-low transitions occur in every received character, the Modem Status Interrupt is generally not useful on the 2710, and programmers will usually want to clear this bit.

Bits 4-7 These bits are always 0.

3.8 MODEM CONTROL REGISTER

Writing to this five-bit register allows the programmer to control the RS-232-C interface outputs of the 8250. A read of the register allows inspection of the control settings.

- | | |
|----------|--|
| Bit 0 | DSR: This bit controls the RS-232-C Data Set Ready line. 1 is the ON state. |
| Bit 1 | CTS: This bit controls the RS-232-C Clear To Send line. 1 is the ON state. |
| Bit 2 | RLSD: This bit controls the RS-232-C Received Line Signal Detect line. 1 is the ON state. |
| Bit 3 | SQD: This bit controls the RS-232-C Signal Quality Detect line. 1 is the ON state. |
| Bit 4 | LOOP: A 1 in this bit enables a loopback feature for testing the 8250 data transfer and interrupt circuitry. Data transmitted is immediately received, being looped directly from the Transmitter Shift Register to the Receiver Shift Register while RxD (SOUT) is held in the marking state and TxD (SIN) is disconnected. Control inputs RTS*, DTR*, DRS*, and AUTOBAUD* are disabled and their circuitry controlled by CTS*, DSR*, RLSD*, and SQD*. The interrupt system, which functions normally except that Modem Status Interrupts are controlled by outputs CTS*, DSR*, RLSD*, and SQD*, can be tested by writing a 1 into any one of the lower six bits of the Line Status Register or the lower four bits of the Modem Status Register. When testing is complete, the Line Control, Modem Control, and Interrupt Identification Registers must be reprogrammed for normal operation and then the Loop Bit must be reset to 0. |
| Bits 5-7 | These bits are always 0. |

3.9 MODEM STATUS REGISTER

The eight bits of this register indicate the state of the RS-232-C control inputs to the 8250 and whether or not these inputs have changed state since their status was last read.

DELTA RTS: A 1 in this bit indicates that interface line RTS has changed state since this register was last read.

DELTA DTR: A 1 in this bit indicates that interface line DTR has changed state since this register was last read.

AUTOBAUD TRAILING EDGE: When this bit is 1, received data input at RI* has gone from a high level to a low level since the register was last read.

DELTA DRS: A 1 in this bit indicates that interface line DRS (Data Rate Select) has changed state since this register was last read.

REQUEST TO SEND

RTS: This bit reflects the RTS interface line. 1 is the ON state.

DATA TERMINAL READY

DTR: This bit reflects the DTR interface line. 1 is the ON state.

AUTOBAUD: This bit reflects the data received from the peripheral. See Section 3.10 for an explanation of its use.

DRS: This bit reflects the DRS (Data Rate Select) interface line.

3.10 AUTO-BAUDING

Auto-bauding is a process whereby the rate at which data transfer will occur is determined by the rate at which a special auto-baud character is received from the control terminal. The 2710 is compatible with the auto-bauding software contained in the CCS MOSS 2.2 Monitor; when the 2710 is used with the CCS 2810 CPU, no extra programming is necessary for auto-bauding any of the 2710's four serial ports.

Users with other monitors may wish to add auto-bauding capability. The monitor must be made to recognize the auto-baud command, jumping to the auto-baud routine when that command is entered. The auto-baud routine may also be called during cold and/or warm starts, as it is by MOSS 2.2. After the auto-baud command, an auto-baud character must be entered; we recommend a carriage return because of the high number of consecutive low bits. The auto-baud routine should poll either bit 2 or bit 6 of the Modem Status register, and when it sees that the AUTOBAUD input has gone low, it should start either a hardware or a software timer (hardware timing is preferable because it is not affected by system clock speeds or wait states). The routine should then poll bit 6 until it goes high again, at which point the timer should be stopped and read. When the length of the sequence of low bits in the auto-baud character is known, it is relatively simple to determine the length of the character, from the length of the character to determine the baud rate, and from the baud rate to determine the necessary divisor to be written to the Baud Rate Divisor Latch.

Because received data is input to the ACE at AUTOBAUD (identified as RI in the 8250 data sheets), Bit 3 of the Modem Status Register will be set to an interrupt condition by every received character. Except in rare instances, programmers will therefore want to disable Modem Status Interrupts.

3.11 RESETTING THE 8250'S

Powering up or resetting the system or the peripherals results in the Master Reset pins of all four ACEs being pulled high. The effect of this on the registers and outputs of the ACEs is summarized in Table 3.6. [Note: ACE outputs OUT 1* and OUT 2* are inverted to control RS-232-C interface lines RLSD and SQD respectively; DSR* and CTS* inverted control DSR and CTS; and SOUT inverted controls RxD. See Section 4.1.3 for further explanation.]

TABLE 3.6. RESET FUNCTIONS

REGISTER	RESET RESULT	SIGNAL	RESET
Interrupt Enable	All bits low	SOUT	High
Interrupt Identification	All bits low	INTRPT (Rcvr Err)	Low
Line Control	All bits low	INTRPT (Data Rcvd)	Low
Modem Control	All bits low	INTRPT (THRE)	Low
Line Status	Bits 0-4, 7 low, bits 5-6 high	INTRPT (Mdm Stat)	Low
Modem Status	Bits 0-3 low, bits 4-7 unaffected	$\overline{\text{CTS}}$	High
Divisor Latch	Unaffected by Reset	$\overline{\text{DSR}}$	High
Receiver Buffer	Unaffected by Reset	$\overline{\text{OUT 1}}$	High
Transmitter Holding	Unaffected by Reset	$\overline{\text{OUT 2}}$	High

3.12 SAMPLE SOFTWARE

The following 8080 code initializes and drives a printer through one of the 2710's serial ports. It is compatible with CP/M 2.2™ and DESPOOL. The HSMSK equate is set for handshaking on RS-232-C pin 4; if handshaking is done on pin 20, then HSMSK EQU 10H. Other values for LBAUD can be selected from Table 3.4. Similar code can be written for other CPUs.

```

;
;
LDATA EQU BASE ;DATA TO BASE ADDRESS
LINTEN EQU BASE+1 ;INTERRUPT ENABLE REGISTER
LIDENT EQU BASE+2 ;INTERRUPT ID REGISTER
LLCTRL EQU BASE+3 ;LINE CONTROL REGISTER
LMDMCT EQU BASE+4 ;MODEM CONTROL REGISTER
LLSTAT EQU BASE+5 ;LINE STATUS REGISTER
LMDMST EQU BASE+6 ;MODEM STATUS REGISTER
LBAUD EQU 0180H ;DIVISOR FOR 300 BAUD
TXMTY EQU 20H ;MASK FOR TRANSMITTER EMPTY
HSMSK EQU 20H ;MASK FOR HANDSHAKE
;
;
; INITIALIZATION CODE
;
MVI A,0FH ;SET HANDSHAKING BITS
OUT LMDMCT
MVI A,83H ;SET DIV LATCH ACCESS
OUT LLCTRL
MVI A,LBAUD/256 ;GET DIV HI BYTE
OUT LINTEN
MVI A,LBAUD MOD 256 ;GET DIV LO BYTE
OUT LDATA
MVI A,3 ;8 BIT WORD, NO PARITY
OUT LLCTRL
XRA A ;ZERO ACCUMULATOR
OUT LINTEN ;DISABLE INTERRUPTS
OUT LLSTAT ;CLEAR STATUS
;
; DRIVER CODE
;
LIST CALL LISTST ;CHECK PRINTER STATUS
JZ LIST ;LOOP IF BUSY
MOV A,C ;GET CHARACTER IN A
OUT LDATA ;OUTPUT TO PORT
RET ;RETURN TO CALLER
;
;
LISTST IN LMDMST ;TEST HANDSHAKE LINE
ANI HSMSK ;ISOLATE HANDSHAKE BIT
RZ ;RETURN IF BUSY
IN LLSTAT ;GET PRINTER STATUS
ANI TXMTY ;ISOLATE TX EMPTY BIT
RZ ;NOT READY: RETURN
ADI 0DFH ;SET A TO OFFH
RET ;READY: RETURN

```


CHAPTER 4

THEORY OF OPERATION

This chapter deals in detail with the hardware design of the 2710, and is meant to be read in conjunction with an examination of the schematic/logic diagram provided in Appendix A. Low-active signals are indicated by an asterisk following the signal name/mnemonic (e.g., RTS*).

4.1 THE SERIAL PORTS

4.1.1 Port Addressing

Each ACE occupies eight consecutive I/O addresses. For a port to be addressed, the corresponding ACE's Chip Select inputs CS0 and CS1 must be high and input CS2* must be low. These three inputs are controlled on the 2710 by the low-byte address and I/O status lines in such a way that the ports: 1) occupy consecutive 8-address blocks whose base address is a multiple of 32; and 2) respond only during I/O cycles.

The base address of the 2710 serial ports is determined by PORT ADDR jumpers 5-7. Each jumper controls whether the corresponding address line (A5-A7) is ex-ORed with a high or a low. Only when each address line is in the state opposite to that of its corresponding jumpered ex-OR input will the open collector output of the three ex-OR gates be high; thus a jumper to ground selects addresses in which the corresponding bit is a 1, while a jumper to +5V selects addresses in which the corresponding bit is a 0. The open

collector output is ANDed with the internal I/O signal (the output of sINP ORed with sOUT) and the resulting signal (PUP = Port Up) is input to each ACE at CS0.

Ace inputs CS1 and CS2* are controlled by address lines A3 and A4. A4 is the CS1 input of Port C and the CS2* input of Port D; its complement, A4*, is the CS1 input of Port A and the CS2* input of Port B. A3 is the CS1 input of Ports B and D and the CS2* input of Ports A and C. The result of this design is that Port A occupies the first eight addresses starting at the base address, Port B occupies the next eight, and so on, as shown in Table 3.1.

4.1.2 Register Control

The ACE register control inputs used on the 2710 are A2, A1, A0, DISTR (Data In Strobe), DOSTR (Data Out Strobe), and MR (Master Reset). Inputs A2, A1, and A0 are controlled by the corresponding address lines and determine which internal register will be accessed. [Note: Because the address bits will always be stable before an ACE is enabled--by sINP or sOUT going high--the ADS* (Address Strobe*) input is not needed and is tied to ground.] A high at DISTR, controlled by sINP, enables reading from a selected register, while a high at DOSTR, controlled by pWR* inverted, enables writing to a selected register. ACE control logic and most of the registers (see Table 3.5 for exceptions) are cleared by a high at MR, which is controlled by the output of SLAVE CLR* ANDed with POC*.

4.1.3 Port Handshaking

The 2710 fully implements the handshaking capabilities of the 8250 ACE in order to provide as complete support of the RS-232-C signals as possible. CTS* and DSR* outputs and RTS* and DTR* inputs control communications link and transmission handshaking; all of these are inverted to produce high-active interface signals. [Note: In 8250 data sheets, inputs and outputs are labeled assuming that the 8250 is Data Terminal Equipment. On the 2710 it functions as Data Communications Equipment. To minimize confusion, we have switched the RTS*, CTS*, DTR*, and DSR* pin labels to be consistent with the interface lines to which they connect.] In addition, the two user-designated control outputs OUT1* and OUT2* have been inverted and tied to

RS-232-C lines RLSD (Receive Line Signal Detect) and SQD (Signal Quality Detect), allowing software control of these handshaking signals. The input RLSD* has been tied to RS-232-C signal DRS (Data Rate Select). This input may be used as defined in RS-232-C (for example, a modem may toggle it to indicate one of two baud rates) or as a general-purpose handshaking line. Finally, transmitted data (from the CPU's point of view) is presented on RxD (named from the DTE point of view), while received data is presented on TxD. Because RS-232-C data transfer employs negative logic, data lines between the ACEs and the interface lines are inverted.

Data on TxD is also inverted and input to the ACE at RI* and is available as an unlatched status bit, AUTOBAUD. This implementation of the RI* input has been made to facilitate Auto-Bauding, for an explanation of which see Section 3.10.

4.1.4 Baud Rate Generator

The 8250 ACE includes the capability of generating virtually any desired baud rate. A clock input, provided on the 2710 by a 1.8432 MHz crystal and associated circuitry, is divided by the number in the Divisor Latch (a 16-bit register allowing divisors from 1 to 65535) to produce an output frequency 16 times the baud rate. This is used internally by the ACE to control transmitter timing and is also output at pin 15, BAUDOUT*. Either BAUDOUT* or a peripherally-generated clock presented on Transmitter Signal Element Timing (DTE) can be jumpered to control receiver timing through the RCLK input. BAUDOUT* is also made available for peripheral timing control on the Receiver Signal Element Timing (DCE) interface line.

4.1.5 Interrupts

The 2710 can be configured to operate in either a polled or a vectored interrupt environment. In a polled environment, the interrupting device pulls S-100 bus line pINT* low. When the CPU acknowledges the interrupt request it looks for a restart vector on the data bus. Because in a polled environment there is no interrupt controller to put a vector on the bus, the CPU reads FFh, the vector for Restart 7. The CPU executes a call to location 0038h, where it must

find a jump to the interrupt handling routine. After saving the necessary registers, the interrupt handling routine must determine which device has interrupted by polling the status of the devices which may be interrupting, after which it must jump to the appropriate interrupt service routine.

In a vectored environment, an interrupt controller monitors the eight lines on the S-100 bus dedicated to vectored interrupts (VI0*-VI7*) and pulls pINT* low whenever one of the VI* lines goes low. When the CPU acknowledges, the interrupt controller places an interrupt vector on the bus; the vector depends on which VI* line has gone active. The CPU then executes a call to one of the eight Restart locations 0-7 as determined by the interrupt vector. Thus vectored interrupts eliminate the need for an interrupt handling routine to poll status in order to determine which device is requesting an interrupt; the Restart locations point directly to the interrupt servicing routines.

The Interrupt Header makes available for simple jumpering all of the lines needed for polled and vectored interrupts: the interrupt request outputs of the four ACEs and S-100 bus lines pINT* and VI0*-VI7*. Whenever a condition occurs for which interrupts have been enabled, an ACE's INTRPT output goes high. The INTRPT outputs from the four ACEs are inverted and tied to four Interrupt Header pins labeled A-D. The eight S-100 Vectored Interrupt bus lines are tied to Interrupt Header pins labeled 0-7; the pINT* bus line is tied to the pin labeled INT. Because the inverters on the INTRPT outputs are open collector, all interrupt request lines may be tied to INT and more than one interrupt request line may be tied to the same vectored interrupt pin. In a vectored environment any port can be made to interrupt over any VI* line, preventing conflicts with existing vectored interrupt assignments.

4.2 THE EPROM

Provision is made on the 2710 for the installation of a 2716-type 2K EPROM, addressable at any 2K boundary within 64K. Each address line A15-A11 is compared with ROM ADDR jumper settings 15-11 in the manner employed for Port Address comparison (described in Section 4.1.1), and when both sMEMR (indicating a memory read cycle) and the open collector output of the five ex-OR gates are high, the ROM is enabled.

Byte-by-byte overlay of the 2710 ROM by indentially

addressed memory located elsewhere in the system is made possible by FF Detect Circuitry. When a ROM location containing all 1's is addressed, the open collector output of the NANDing of the data lines (FFD*) goes low, disabling the Data In Buffer (see Section 4.4) and thereby allowing other memory with the same address to place data on DI0-7.

4.3 DATA BUFFERS

S-100 bus lines DO0-7 and DI0-7 are buffered by U35 and U36 respectively and tied to the 2710's bi-directional data bus. The Data Out buffer is enabled when the output of the NANDing of SOUT and PUP is low; this ensures that data is allowed onto the board only when a 2710 port is transmitting. The Data In buffer is enabled by a low output from the NANDing of pDBIN and FFD*. FFD* is low whenever all 1's are present on the 2710's data bus (see Section 4.2), which is the case in all read cycles in which neither a 2710 register nor a programmed on-board memory location is being read.

APPENDIX A

TECHNICAL INFORMATION

A.1 SPECIFICATIONS

SIZE:

Board: 10" long x 5" wide
Connector: 6.365" long x .3" wide;
2.125" from right of board
Component Ht: less than .5"

POWER SUPPLY:

+8 Volts Regulated On-Board to +5 Volts
+16 Volts Regulated On-Board to +12 Volts
-16 Volts Regulated On-Board to -12 Volts
Consumption: 750mA at +8 V.
150mA at +16 V.
100mA at -16 V.
Heat Burden: 132 gram-calories/minute
.87 BTU/minute

ENVIRONMENTAL REQUIREMENTS:

Temperature: 0'C. to +70'C.
Humidity: up to 90%

INTERFACE:

Processor: S-100 Bus Conforms to IEEE Standards
Jumper-Selectable Port Base Address
Peripherals: Four 13x2 Connectors
RS-232-C Compatibility
Modem Control Handshaking
Jumper-Selectable External Rx Clock

MEMORY:

Circuitry, Socket for 2K ROM: 2716-type
Jumper-Selectable Base Address
1 Byte to 2K Byte Overlay Using FF Detect

ADDITIONAL FEATURES:

Reliable, easy-to-configure Berg jumper plugs
Low-power Schottky and MOS devices for minimum
power consumption
Sockets for all ICs
Fiberglass epoxy (FR-4) PC board
Solder-masked both sides
Gold-plated connector fingers
Silk-screened component outlines, part designation,
reference numbers

A.2 8250 ACE PINOUTS

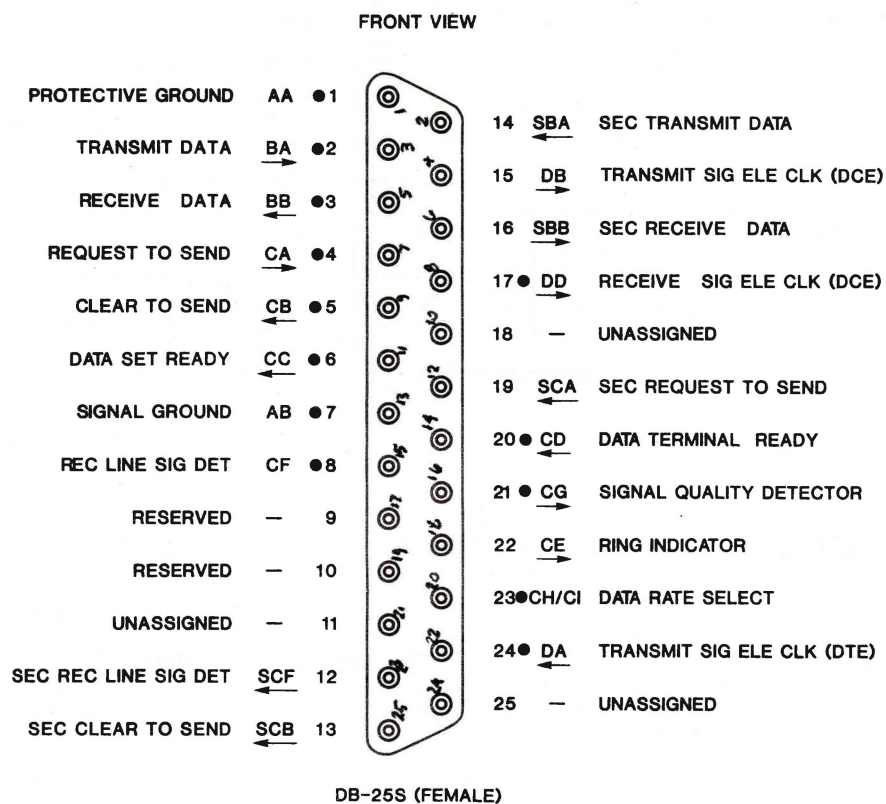
8250 ACE
PINOUTS

D0	1	40	VCC
D1	2	39	RI*
D2	3	38	RLSD*
D3	4	37	DTR*
D4	5	36	RTS*
D5	6	35	MR
D6	7	34	OUT1*
D7	8	33	DSR*
RCLK	9	32	CTS*
SIN	10	31	OUT2*
SOUT	11	30	INTRPT
CS0	12	29	NC
CS1	13	28	A0
CS2*	14	27	A1
BAUDOUT*	15	26	A2
XTAL1	16	25	ADS*
XTAL2	17	24	CSOUT
DOSTR*	18	23	DDIS
DOSTR	19	22	DISTR
VSS	20	21	DISTR*

A.3 INTERFACE CONNECTOR PINOUTS

PROTECTIVE GROUND	AA	● 1	2 ●	
TRANSMIT DATA	BA	● 3	4 ●	
RECEIVE DATA	BB	● 5	6 ●	
REQUEST TO SEND	CA	● 7	8 ●	CG RECEIVER SIG EL TIMER (DCE)
CLEAR TO SEND	CB	● 9	10 ●	
DATA SET READY	CC	● 11	12 ●	
SIGNAL GROUND	AB	● 13	14 ●	CD DATA TERMINAL READY
REC LINE SIG DET	CF	● 15	16 ●	DD SIG QUALITY DETECT
		● 17	18 ●	
		● 19	20 ●	CH/CI DATA RATE SELECT
		● 21	22 ●	DA TRANSMIT SIG EL TIMER (DTE)
		● 23	24 ●	
		● 25	26 ●	

A.4 RS-232-C CONNECTOR PINOUTS



• These lines supported by the 2710

A.5 DEFINITION OF RS-232-C INTERFACE CONFIGURATIONS

A	Transmit Only
B	Transmit Only*
C	Receive Only
D	Half Duplex; or Duplex*
E	Full Duplex
F	Primary Channel Transmit Only* / Secondary Channel Receive Only
G	Primary Channel Receive Only / Secondary Channel Transmit Only*
H	Primary Channel Transmit Only / Secondary Channel Receive Only
I	Primary Channel Receive Only / Secondary Channel Transmit Only
J	Primary Channel Transmit Only* / Half Duplex Secondary Channel
K	Primary Channel Receive Only / Half Duplex Secondary Channel
L	Half Duplex Primary Channel / Half Duplex Secondary Channel; or
L	Duplex Primary Channel* / Duplex Secondary Channel*
M	Duplex Primary Channel / Duplex Secondary Channel
Z	Special (Circuits specified by supplier)

* Note the inclusion of Request to Send in a Transmit Function, where it would not ordinarily be expected, but could indicate a non-transmit mode to the data communications equipment (DCE) to permit it to remove a line signal or to send synchronizing or framing signals as required.

A.6 SIGNAL CHART FOR RS-232-C INTERFACE CONFIGURATIONS

Interchange Circuit		Interface Configuration															
		A	B	C	D	E	F	G	H	I	J	K	L	M	Z		
AA	Protective Ground	-	-	-	-	-	-	-	-	-	-	-	-	-	-		
AB	Signal Ground / Common Return	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
BA	Transmitted Data	X	X		X	X	X		X		X		X	X	X		
BB	Received Data			X	X	X		X		X		X	X	X	X		
CA	Request to Send		X		X		X				X		X		X		
CB	Clear to Send	X	X		X	X	X		X		X		X	X	X		
CC	Data Set Ready	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
CD	Data Terminal Ready	S	S	S	S	S	S	S	S	S	S	S	S	S	S		
CE	Ring Indicator	s	s	s	s	s	s	s	s	s	s	s	s	s	s		
CF	Received Line Signal Detector			X	X	X		X		X		X	X	X	X		
CG	Signal Quality Detector																
CH/CI	Data Signalling Rate Selector (DTE/DCE)																
DA/DB	Transmit Signal Element Timing (DTE/DCE)	T	T			T	T	T		T		T	T	T	T		
DD	Receiver Signal Element Timing (DCE)			t	t	t		t		t		t	t	t	t		
SBA	Secondary Transmitted Data							x		x	x	x	x	x	x		
SBB	Secondary Received Data							x	x		x	x	x	x	x		
SCA	Secondary Request to Send							x			x	x	x				
SCB	Secondary Clear to Send							x		x	x	x	x	x	x		
SCF	Secondary Received Line Signal Detector							x	x		x	x	x	x	x		

Upper case indicates a line supported by the CCS 2710.

Lower case indicates a line not supported by the CCS 2710.

X = Basic interchange circuits, all systems

T = Additional interchange circuits required for synchronous channel

S = Additional interchange circuits required for switched service

0 = Specified by supplier as required

- = Optional; supported by the CCS 2710

A.7 PARTS LIST

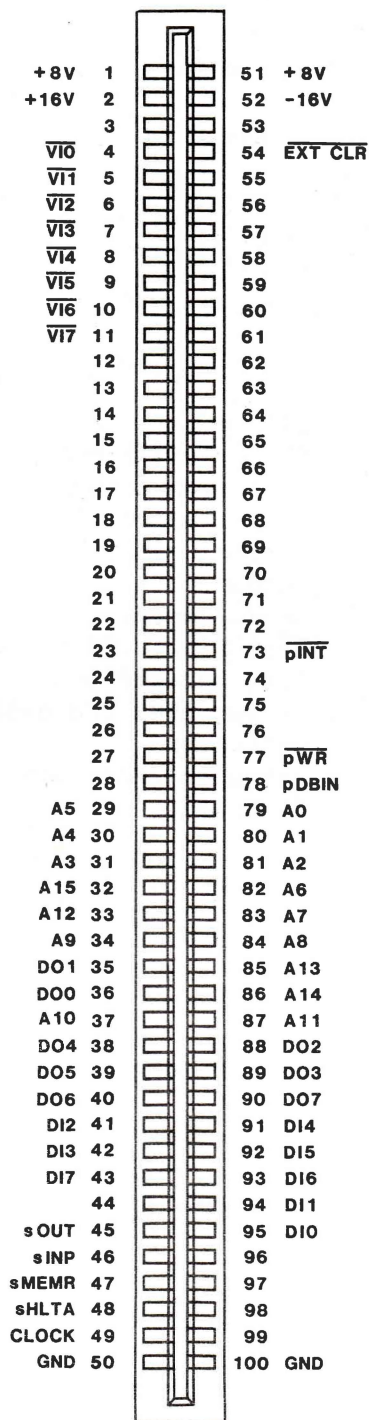
QTY	REF	DESCRIPTION	CCS PART #
INTEGRATED CIRCUITS			
1	U29	74LS00 quad 2-in NAND	30000-00000
1	U39	74LS04 hex inverters	30000-00004
1	U28	74LS05 hex inverters, OC	30000-00005
1	U38	74LS08 quad 2-in AND	30000-00008
1	U37	74LS30 8-in NAND	30000-00030
1	U34	74LS32 quad 2-in OR	30000-00032
2	U30-31	74LS136 quad ex-OR	30000-00136
3	U32,35-36	74LS244 tri-state buffer	30000-00244
14	U2,8-10,14-20, 23,25-26	75150 line driver	30300-00150
6	U1,3,11-12, 21-22	75154 line receiver	30300-00154
1	U27	7805 +5 V regulator	32000-07805
1	U13	7812 +12 V regulator	32000-07812
1	U24	7912 -12 V regulator	32000-07912
4	U4-7	MOS 8250 ACE	31200-08250
CAPACITORS			
22	C1-11,13-14, 16-19,24-28	.1 uf, mono	42034-21046
6	C12,15,20-23	4.7 uf, tantalum	42804-54756
1	C30	.01 uf, ceramic	42142-21036
1	C29	20 pf, dipped mica	42215-52005
RESISTORS			
1	R5	220 ohm, 1/4 W, 5%	40002-02215
2	R6-7	1K ohm, 1/4 W, 5%	40002-01025
1	R8	2.7K ohm, 1/4 W, 5%	40002-02725
2	R9-10	470 ohm, 1/4 W, 5%	40002-04715
1	RP1	2.7K ohm x 7 SIP	40930-72726

QTY	REF	DESCRIPTION	CCS PART #
SOCKETS			
14	XU2,8-10,14-20,23,25-26	8 pin DIP	58102-00080
8	XU28-31,34,37-39	14 pin DIP	58102-00140
7	XU1,3,11-12,21-22,XJ1	16 pin DIP	58102-00160
3	XU32,35-36	20 pin DIP	58102-00200
1	XU33	24 pin DIP	58102-00240
4	XU4-7	40 pin DIP	58102-00400

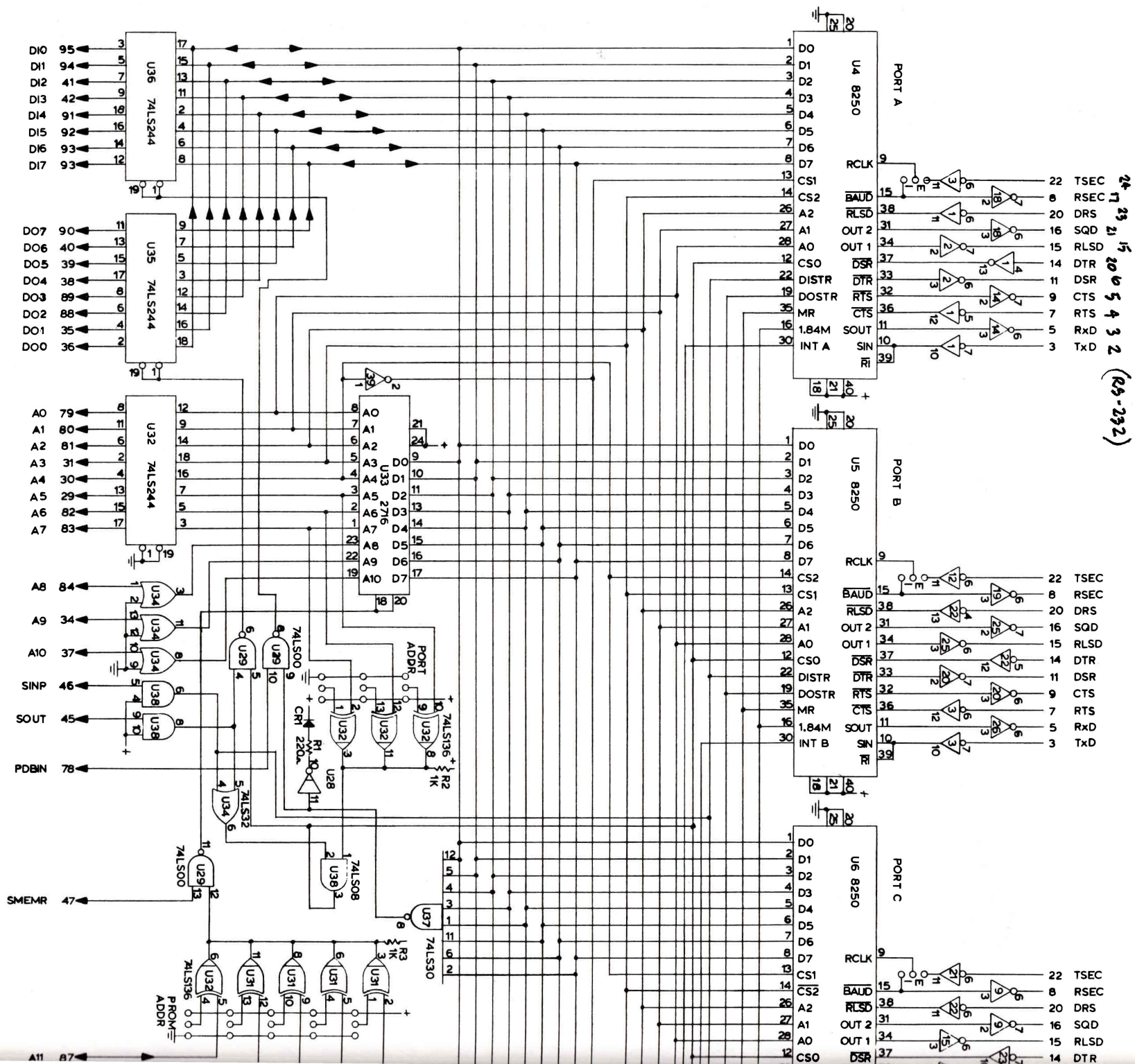
MISCELLANEOUS

1	CR1	LED, red	37400-00001
1	X1	XTAL, 1.8432 MHz	48132-84321
4		Keyed Connector, 2 x 13	56004-02013
1	J1	Keyed Header, 2 x 8	55000-10000
1	J1	Header Cover, 2 x 8	55000-10001
12		Header, 1 x 3	56004-01003
12		Berg Jumpers	56200-00001
1	XU27	Heat Sink, .5" blk anodized	60022-00001
3		Nut, hex KEP 6-32	73006-32001
3		Screw, SEMS PPH 6-32 x 5/16	71006-32051
2		Extractor	60010-00001
2		Extractor roll pin	60010-00000
1		PC Board	02710-00002

A.8 2710 BUS CONNECTOR PINOUT

C
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M
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TOP VIEW



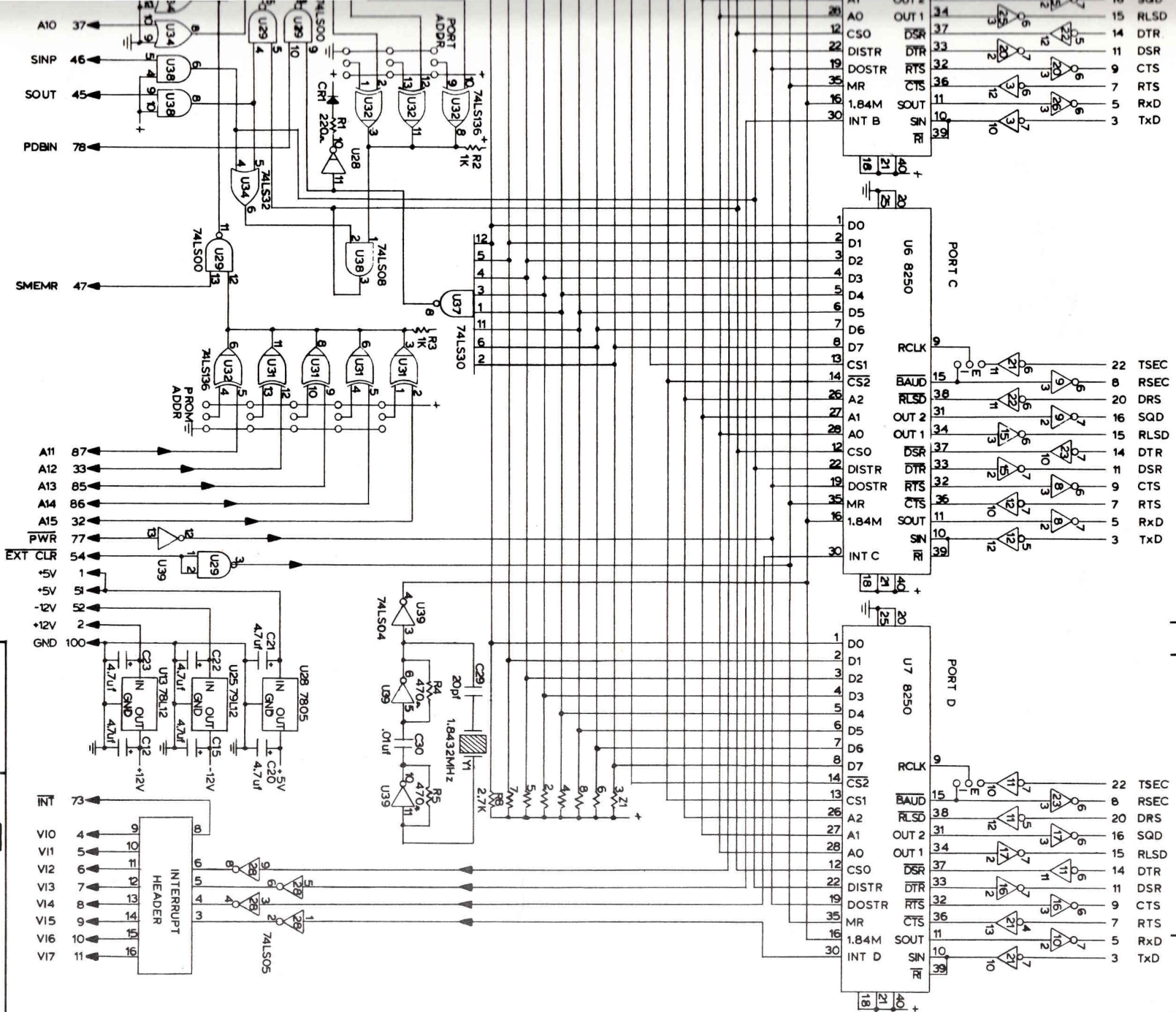
REVISIONS

LTR

DESCRIPTION

DATE

APPROVED



California Computer Systems

Model 2710

TOLERANCES UNLESS OTHERWISE SPECIFIED	
±	±
APPROVALS	DATE
DESIGNED BY	1-19-81
CHECKED	

SCALE
FULL
SIZE
DRAWING NO.

DO NOT SCALE DRAWING

SHEET 1 of 1

