ads

NOISEMAKER II ©

MANUAL

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I. INTRODUCTION

The AY-3-8910 programmable sound generator (PSG) is a large scale integrated circuit which can produce a wide variety of complex sounds under software control. After initialization of the registers in the PSG, sounds can continue to be produced while allowing the processor to do other tasks.

Each AY-3-8910 has three 12 bit tone generators: one 4 bit amplitude control for each of the three tone sources, one 5 bit noise generator, and one 16 bit envelope generator. As an added feature, the AY-3-8910 has two I/O ports which are brought out for user applications.

The techniques described in this manual will produce a wide variety of results. However, since the range of sounds to be synthesized are so vast, this manual should only be viewed as an introduction to the capabilities of the ADS NOISEMAKER I.

II. BOARD CONSTRUCTION

1. Begin construction of the ADS NOISEMAKER I by first examining it for obvious shorts. If an ohmmeter is available measure between address lines, data lines, and the + 5 volt and ground for shorts.

2. Noting the orientation against the silk screen, install and solder the I/C sockets. No socket should be used for the dip switch S1.

3. Carefully observing the polarized capacitors orientation against the silk screen, install and solder the capacitors.

4. The dip switch S1 and resistors should be installed next.

5. The +5 volt regulator should be installed next. Using heat sink compound sparingly, mount the regulator to the heat sink and board with a 6-32 x 3/8 screw and nut.

6. Apply power to the board and verify that between 4.8 and 5.2 volts are available to the I/C's on the board. ie. U3 pin 40.

7. Remove power and install the I/C's (do not bend any pins and/or reverse the I/C's in their sockets.)

8. Connect two 8 ohm speakers to output connector J2. (speaker pins for PSG U3 are J2/16&15 and speaker pins for U8 are J2/13&14.

9. The ADS NOISEMAKER I is designed to work in a 1 MHz system. For use in faster systems an onboard wait state generator has been incorporated using I/C's U15 & U16. With these I/C's in their sockets the NOISEMAKER I will default to zero wait states dictated by the default trace placed on the P.C. board. (note schematic P.9) If you require one or two wait states for 2 or 4 MHz systems cut the default trace with a knife and install the necessary jumper using the pads on the board. A jumper between the pad labeled 1 on the P.C. board and the wait state common terminal will generate one wait state. Similarly 2 wait states can be generated by using the pad labeled 2. Keep in mind that after the default trace has been cut you must install one jumper wire in the appropriate location.

10. Your NOISEMAKER I is now ready to be tested in your system. Select the group of four I/O addresses you want the board to respond to (note diagram 1). They are set with the 6 position dip switch S1, with the switch nearest the top of the board setting the most significant bit. A closed switch represents a logic Ø.

Diagram 1

8080 I/O Addresses — S7, S6, S5, S4, S3, S2 — Board address 0,4,8,.... 248,252 select

A1 — PSG select 0-PSG(A); 1-PSG(B)

AØ — PSG register 0-address (write only) 1-data (read/wri

11. Set volume R7 and R18 midway.

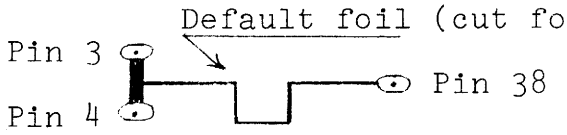
12. Install the board and verify that your computer and other I/O devices function normally.

III. HELPFUL HINTS

Your NOISEMAKER I may be operated with only one speaker if desired simply by omitting I/C U14, resistors R8,R9,R15,R18 and capacitors C2, C3,C18,&C20, then connecting a jumper wire between the pad that is for the +(positive) lead of C2 and the + lead of C17. If you follow the copper trace from the + lead of C17 you will find an open feed through hole which is convenient to solder to. With the above modifications your NOISEMAKER I will work with both PSG's driving audio amp U2 which has its output available at J2 pins 16 & 15.

To further allow you total use of the capabilities on the AY-3-8010 a default foil (note schematic P. 9) connecting analog output pins 3&4 to analog output pin 38 on both U3 & U8 has been incorporated. These foil traces may be found on the bottom side of the P.C. board near their respective AY-3-8910 I/C and designated by a notch as described in diagram 2 below. By cutting either or both of the traces the channel C four bit D/A converters become available for user applications. Keep in mind that after the trace is cut the channel C tone and noise generator will no longer be available to the audio amplifiers. If you no longer wish to use the D/A converter then a jumper wire may be installed to bring the NOISEMAKER back to its origional configuration.

Diagram 2



IV. USING THE ADS NOISEMAKER I

The AY-3-8910 is programmad through two I/O addresses. before one of the sixteen internal registers can be read from or written to, it must first be selected by writing a number (0-15) into the PSG Address register. (Diagram 2a page 3) The selected data register can then be read from or written to until another PSG data register is selected.

Diagram 2a - Address Register (Pointer Register)

B7	B6	B5	B4	B3	B2	B1	B0

HIGH ORDER LOW ORDER

The four low order address bits (B3-B0) select one of 16 Data registers (R0-R15). The four High order address bits (B7-B4) are not used. In the B7-B4 locations, the address register will only recognize 0000. To produce a tone, you must:

1) Select the enables register (7)
2) Load it with ØFEH (Tone out Ch.A)
3) Select the Ch. A Amplitude Register (8)
4) Load it with ØFH (Max. Output)
5) Select the Ch. A Fine Tune Register (Ø)
6) Load it with Ø8ØH (Audible Frequency)

```
MVI  A, #Ø7
OUT  NOISEMAKER
MVI  A, #ØFEH
OUT  NOISEMAKER + 1
MVI  A, #Ø8
OUT  NOISEMAKER
MVI  A, #ØFH
OUT  NOISEMAKER + 1
MVI  A, #00
OUT  NOISEMAKER
MVI  A, #80H
OUT  NOISEMAKER + 1
```

```
MVI  A, #Ø7
OUT  NOISEMAKER + 2
MVI  A, #ØFEH
OUT  NOISEMAKER + 3
MVI  A, #Ø8
OUT  NOISEMAKER + 2
MVI  A, #ØFH
OUT  NOISEMAKER + 3
MVI  A,#ØØ
OUT  NOISEMAKER + 2
MVI  A, #80H
OUT  NOISEMAKER + 3
```

The data register is a Read/Write register but efforts must be taken to mask off any "not used" bits when reading from the data register. General Instruments does not guarantee "not used" bits to be at logic "0".

V. ARCHITECTURE AND EQUATIONS GOVERNING THE PSG

(a) TONE GENERATOR CONTROL

The frequency of each square wave generated by the three tone generators (Channels A, B and C) is obtained in the PSG by first counting down the input clock by 16, then by further counting down the result by the programmed 12 bit tone period value. Each 12 bit value is obtained in the PSG by combining the contents of the relative Course and Fine Tune Register illustrated in Fig. 1, page 8 and Diagram 3 below.

Diagram 3

				COARSE TUNE				FINE TUNE							
B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2	B1	B0
Not Used				TP 11	TP 10	TP 9	TP 8	TP 7	TP 6	TP 5	TP 4	TP 3	TP 2	TP 1	TP 0

12 Bit Tone Period (TP) to Tone Generator

The equations listed below define tone frequency.

Tone Frequency $f_t = f_{clock} / (16 * TP10)$ where f_{clock} = frequency of clock (Note Schematic on Page 9

Eq. 3 $TP_{10} = 256\ CT_{10} + FT_{10}$ (Decimal equivalent of Tone Period)

CT_{10} defines the decimal equivalent of Coarse Tune Reg.

FT_{10} defines the decimal equivalent of Fine Tune Reg.

(b) **NOISE GENERATOR CONTROL** (Register R6)

The frequency of the noise source is obtained in the PSG by first counting down the input clock by 16, then by further counting down the result by the programmed 5 bit noise period value. This 5 bit value consists of the lower 5 bits (B4-B0) of Register R6. (Illustrated in Diagram 4 below.)

Diagram 4

Register R6

B7	B6	B5	B4	B3	B2	B1	B0
NOT USED			5 Bit Noise Period (NP)				

Note: The 5 bit value in R6 is a period value. Therefore, the higher the value in the register, the lower the resultant noise frequency.

Eq. 4 Noise Frequency $F_n = f_{clock} / (16NP_{10})$

NP defines decimal equivalent of the Noise Period Register.

(c) **ENABLE CONTROL** (Register R7)

This is a multi-function register which controls the three noise/tone mixers and two general purpose I/O ports.

The mixers as noted above combine the noise and tone frequencies for each of the three channels. The determination of combining neither, either, or both noise and tone frequencies on each channel is made by the state of bits B5-B0 of R7. (See Diagram 5 below.)

Diagram 5

Register R7

B7	B6	B5	B4	B3	B2	B1	B0
$\overline{\text{Input Enable}}$		$\overline{\text{Noise Enable}}$			$\overline{\text{Tone Enable}}$		
B	A	C	B	A	C	B	A

Note: These Registers are Negativ True

The direction (In or Out) of the two general purpose I/O ports (IOA and IOB) is determined by the state of bits B7 and B6 of R7.

A logic level of "0" entered in the Noise and/or Tone Enable Register will activate the noise and/or tone for that channel. A logic level of "1" entered in the Noise and/or Tone Enable Register will deactivate that noise and/or tone.

A logic level of "0" written into the I/O Enable Register will place that/those ports into the input mode. A logic level of "1" written into the Input Enable Register will place that/those ports into the output mode.

Note that the disabling noise and tone does not turn off a channel. A high frequency envelope would be heard as a tone or a series of clicks. Turning a channel off can only be accomplished by writing zeroes into the Amplitude Control Registers described next.

(d) AMPLITUDE CONTROL

The amplitudes of the signals generated by each of the three D/A converters (one for each channel) is determined by the contents of the lower 5 bits (B4-B0) of Registers R8, R9 and R10. (See Fig. 1, Page 8.)

M-0 Amplitude is fixed at one of 16 levels as determined by L3, L2, L1 and L0

M-1 Amplitude is variable at 16 levels as determined by the output of the generator. (Note Fig. 3, Page 8.)

(e) ENVELOPE PERIOD CONTROL

To accomplish the generation of fairly complex envelope patterns, two independent methods of control are provided in the PSG. First, it is possible to vary the frequency of the envelope using Registers R11 and R12 and second, the relative shape and cycle pattern of the envelope can be varied using Register R13. The following paragraphs first describe the envelope period control and then the envelope shape/cycle control.

The frequency of the envelope is obtained in the PSG by first counting down the input clock by 256, then by further counting down the result by the programmed 16 bit envelope period value. This 16 bit value is obtained in the PSG by combining the contents of the Envelope Coarse and Fine Tune Registers. (See Diagram 6 below.)

Diagram 6

R12 - COARSE TUNE REGISTER								R11 - FINE TUNE REGISTER							
B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2	B1	B0

EP 15	EP 14	EP 13	EP 12	EP 11	EP 10	EP 9	EP 8	EP 7	EP 6	EP 5	EP 4	EP 3	EP 2	EP 1	EP 0

16 Bit Envelope Period (EP)

Note that the 16 bit value programmed in the combined Coarse and Fine Tune Registers is a period value; therefore, the higher the value in the register, the lower the resultant envelope frequency.

Eq. 5 Envelope Frequency $F_e = f_{clock} / 256\ EP_{10}$

$EP_{10} = 256\ CT_{10} + FT_{10}$ (Decimal Equivalent of Envelope Period)

CT_{10} defines the decimal equivalent of the Coarse Tune Register

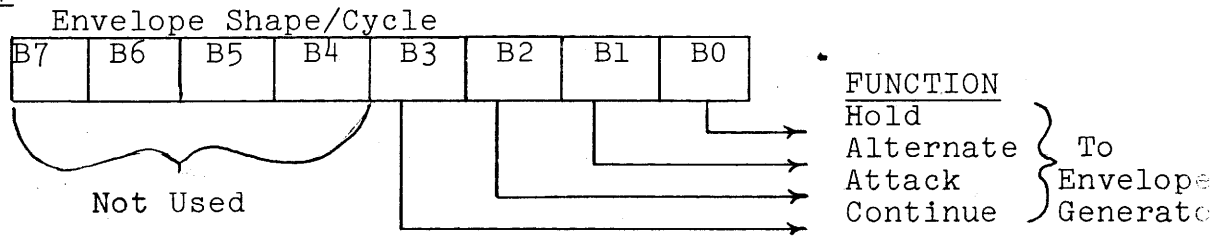
FT_{10} defines the decimal equivalent of the Fine Tune Register

(f) ENVELOPE SHAPE/CYCLE CONTROL

The envelope generator further counts down the envelope frequency by 16, producing a 16 state per cycle envelope pattern as defined by its 4 bit counter output, E3, E2, E1, and E0. The particular shape and cycle pattern of any desired envelope is determined by controlling the count pattern (count up/count down) of the 4 bit counter and by defining a single-cycle or repeat-cycle pattern.

This Envelope Shape/Cycle Control is contained in the lower 4 bits (B3-B0) of Register 13. Each of these 4 bits controls a function in the envelope generator. (See Diagram 7 below.)

Diagram 7



ENVELOPE SHAPE/CYCLE DEFINITIONS

HOLD — When Logic "1", limits the envelope to one cycle, holding the last count of the envelope counter (E3-E0=0000 or 1111) depending on whether the envelope counter was in a count down or count up mode.

ALTERNATE — When Logic "1", the envelope counter reverses count direction (up-down) after each cycle.

ATTACK — When Logic "1", the envelope counter will count up (attack) from E3, E2, E1, E0 = 0000 to E3, E2, E1, E0 = 1111; when Logic "0", the envelope counter will count down (decay) from E3, E2, E1, E0 = 1111 to E3, E2, E1, E0 = 0000.

CONTINUE — When set to Logic "1", the cycle pattern will be as defined by the hold bit. When set to Logic "0", the envelope generator will reset to 0000 after one cycle and hold at that count.

Figure 2 on page 8 gives a graphic representation of the possible envelope shapes.

Note: When both the hold bit and the alternate bit are "1's", the envelope is reset to its initial count before holding.

(g) I/O PORTS

Registers R14 and R15 function as intermediate data storage registers between the PSG/CPU data bus (D0-D7) and the two I/O ports. (IOA7-IOA0 and IOB7-IOB0) Both ports are made available to the user via a 16 pin dip connector. (Note Schematic on page 9.) Using the I/O Register for data transfer will have no effect on sound generation.

To output data from the CPU bus to a peripheral deveice connected to I/O Port A requires the following steps:

1. Latch Address R7 (Select Enable Register)
2. Write Data to PSG (Setting B6 of R7 to "1")
3. Latch Address R14 (Select IOA Register)
4. Write Data to PSG (Data to be Output on I/O Port A)

To input data from I/O Port A to the CPU bus requires the following steps:

1. Latch Address R7 (Select Enable Register)
2. Write Data to PSG (Setting B6 of R7 to "0")
3. Latch Address R15 (Select IOA Register)
4. Read Data From PSG (Data From I/O Port A)

When left in the output mode, data will remain on the I/O port(s) until changed by loading different data or by resetting the PSG.

When left in the input mode, the contents of Register R14 and R15 will follow the signals applied to the I/O ports; however, transfer of this data to the CPU requires a "Read" operation.

(h) D/A CONVERTER OPERATION

Since we are trying to produce sounds for the non-linear amplitude detection mechanism of the human ear, the D/A conversion is preformed in logarithmic steps with a normalized voltage range from 0 to 1 volt. The specific amplitude control of each of the three D/A converters is accomplished by the three sets of 4 bit outputs of the amplitude control block. The mixer outputs provide the base signal frequency. (Noise and Tone)

REG. \ BIT	B7	B6	B5	B4	B3	B2	B1	B0
R0 Channel	8 Bit Fine Tune A							
R1 A Tone					4 Bit Coarse			
R2 Channel	8 Bit Fine Tune B							
R3 B Tone					4 Bit Coarse			
R4 Channel	8 Bit Fine Tune C							
R5 C Tone					4 Bit Coarse			
R6 Noise Per.				5 Bit Period				
R7 Enable	IN/OUT		Noise			Tone		
	IOB	IOA	C	B	A	C	B	A
R8 Amplitude A				M	L3	L2	L1	L0
R9 Amplitude B				M	L3	L2	L1	L0
R10 Amplitude C				M	L3	L2	L1	L0
R11 Envelope	8 Bit Fine Tune							
R12 Period	8 Bit Coarse Tune							
R13 Envl Shape					CONT	ATT	ALT	HOLD
R14 I/O Port A	8 Bit Parallel I/O Port							
R15 I/O Port B	8 Bit Parallel I/O Port							

Fig. 1 PSG Register Array

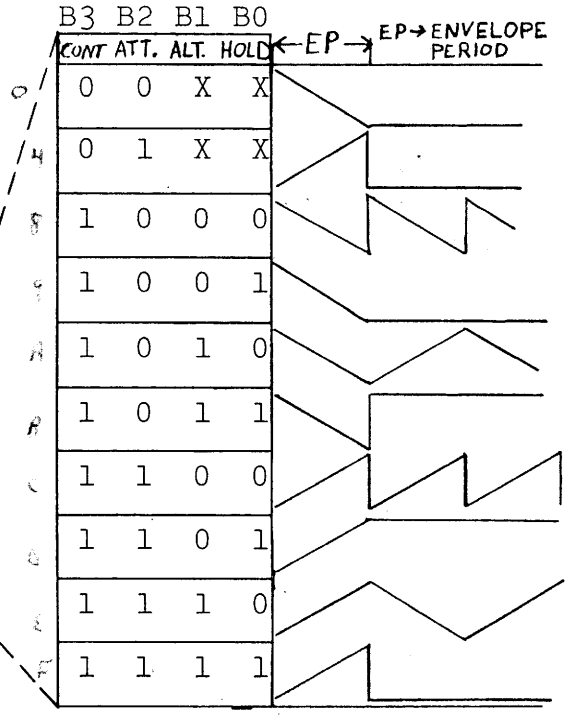


Fig. 2 Envelope Shape

Equations

Tone Frequency $f_T = f_{clock}/(16TP_{10})$ Where: f_{clock} = frequency of clock to 8910

$TP_{10} = 256CT_{10} + FT_{10}$ = Decimal Equivalent of Tone Period
CT_{10} = Decimal Equivalent of Coarse Tune Register
FT_{10} = Decimal Equivalent of Fine Tune Register

Noise Frequency $f_N = f_{clock}/(16NP_{10})$ Where:

NP_{10} = Decimal Equivalent of the Noise Period Register

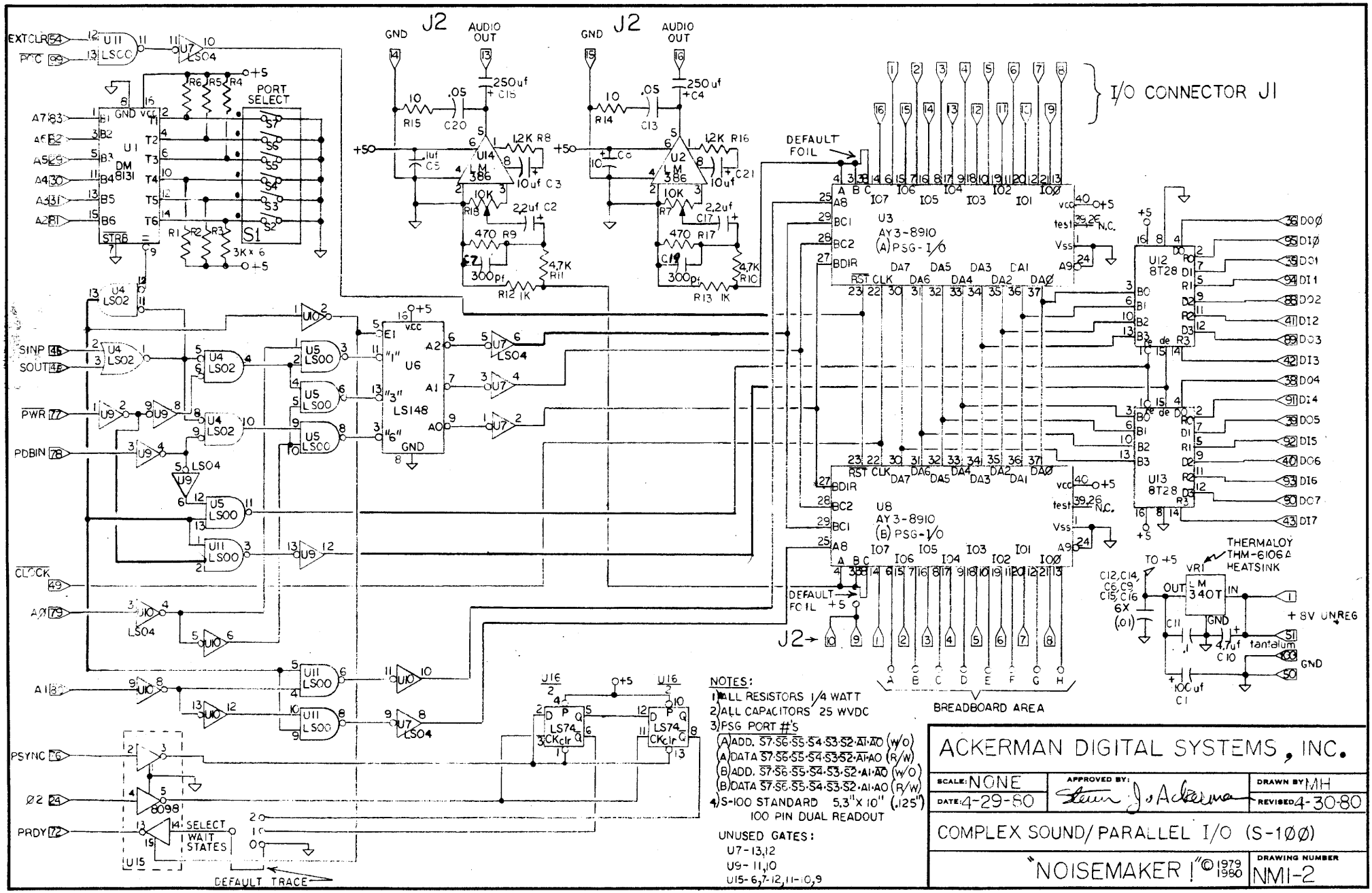
Amplitude Control:

M=0 Amplitude is fixed at one of 16 levels as determined by L3, L2, L1 & L0.
M=1 Amplitude is variable at 16 levels as determined by the output of the envelope generator.

Envelope Frequency $f_E = f_{clock}/256EP_{10}$ Where: $EP_{10} = 256CT_{10}+FT_{10}$

CT_{10} = Decimal Equivalent of the Coarse Tune Register Bits B7 Thru B
FT_{10} = Decimal Equivalent of the Fine Tune Register Bits B7 Thru B0

Note: When reading from a PSG register with less than 8 Bits, care must be taken to mask the unused bits to insure the data is read accuratly.



NOTES:
1) ALL RESISTORS 1/4 WATT
2) ALL CAPACITORS 25 WVDC
3) PSG PORT #'S
   A) ADD. $\overline{S7}\cdot\overline{S6}\cdot\overline{S5}\cdot\overline{S4}\cdot\overline{S3}\cdot\overline{S2}\cdot A1\cdot\overline{A0}$ (W/O)
   A) DATA $\overline{S7}\cdot\overline{S6}\cdot\overline{S5}\cdot\overline{S4}\cdot\overline{S3}\cdot\overline{S2}\cdot A1\cdot A0$ (R/W)
   B) ADD. $\overline{S7}\cdot\overline{S6}\cdot\overline{S5}\cdot\overline{S4}\cdot\overline{S3}\cdot\overline{S2}\cdot A1\cdot\overline{A0}$ (W/O)
   B) DATA $\overline{S7}\cdot\overline{S6}\cdot\overline{S5}\cdot\overline{S4}\cdot\overline{S3}\cdot\overline{S2}\cdot A1\cdot A0$ (R/W)
4) S-100 STANDARD 5.3" X 10" (.125")
   100 PIN DUAL READOUT

UNUSED GATES:
U7-13,12
U9-11,10
U15-6,7-12,11-10,9

ACKERMAN DIGITAL SYSTEMS, INC.

SCALE: NONE	APPROVED BY: Steven J. Ackerman	DRAWN BY: MH
DATE: 4-29-80		REVISED 4-30-80

COMPLEX SOUND/PARALLEL I/O (S-100)

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8T28 CROSS REFERENCE:

Signetics	NE 8T28
Motorola	MC 8T28 MC 6889
American Micro Devices	AM8T28

8T26A's may be substituted by inverting with software.

8T26A CROSS REFERENCE:

Motorola	MC 6880
Texas Instruments	SN 75136

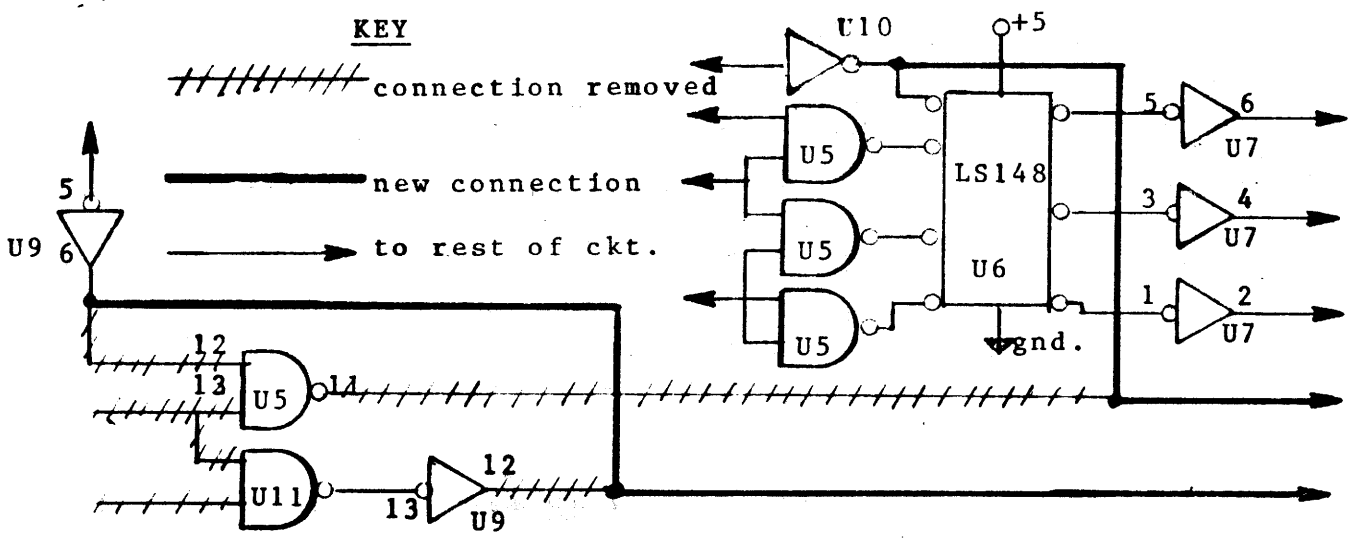
If you are unable to locate 8T28's or 8T26, the following modifications will allow you to use the (currently) more available 8216's.

MODIFICATIONS:

1). On I.C. U5 bend pins, 11, 12 and 13 up and out of socket.
2). On I.C. U9 bend pins 12 up and out of the socket.
3). On I.C. U11 bend pins, 1, 2 and 3 up and out of the socket.
4). Install the following jumpers:

a). U5 pin 11 (on solder side of PCB) to U10 pin 2
b). U9 pin 6 to U9 pin 12 (solder side of PCB)

Our engineers advise that under certain rare circumstances; the above mod may be subject to race conditions. While this is generally not a problem it should be borne in mind.



PART	DESCRIPTION	QUANTITY	NUMBER
*74LS74	dual D latch	1	U16
*8098 or 8T98	inverting buffer	1	U15
✓74LS02	quad nor	1	U4
**8T28	data line XCVR	2	U12,U13
✓AY-3-8910	GI sound generator	1 or 2	U3,U8
LM386N	audio amplifier	2	U2,U14
✓74LS04	TTL hex inverter	3	U7,U9,U10
✓74LS00	TTL quad nand	2	U5,U11
74LS148	priority encoder	1	U6
DM8131	hex comparator	1	U1
CTS 206-6	6 position dip switch	1	S1
****MC7805	+5 volt regulator	1	VR1
.01uf 25V.	filter capacitor	6	C6,C9,C12 C14,C15,C16
.05uf 25V.	capacitor	2	C13,C20
0.1uf 25V.	filter capacitor	2	C5,C11
4.7uf 25V.	Tantalum capacitor	1	C10
2.2uf 25V.	A.C. coupling cap.	2	C2,C17
10 uf 25V.	electrolytic	3	C3,C8,C21
250uf 25V.	A.C. coupling cap.	2	C4,C18
300pf 25V.	capacitor	2	C7,C19
100uf 25V.	electrolytic	1	C1
***3000 ohm	pull up resistor	6	R1 thru R6
1000 ohm	current divider	2	R12,R13
39K ohm	summing junction	2	R10,R11
10 ohm	resistor	2	R14,R15
4.7K ohm	resistor	2	R9,R17
1.2K ohm	resistor	2	R8,R16
10K ohm	P.C. mount trim pot	2	R7,R18
I.C. socket	8 pin solder tail	2	
I.C. socket	14 pin solder tail	7	
I.C. socket	16 pin solder tail	7	
I.C. socket	40 pin solder tail	1 or 2	

*If you are using the Noisemaker I in a 1MHZ System, the wait state generator I/C's U15 & U16 may be omitted to save on component count. The unit will automatically default to zero wait states without these parts.

**8T26 may be substituted for 8T28's with inverting software.

***All resistors 1/4 watt, unless otherwise specified.

****Use Thermalloy heat sink THM6106-14.