ACOM/Electronics
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8088 PROCESSOR BOARD
P188

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SHIPPING CONFIGURATION

The P188 card S/N _____ was shipped from the factory with the following configurations:

( ) Slave processor jumper

( ) Master processor jumper

( ) Shared processor jumper

( ) Sync and M1 jumpered for dynamic memory operation as outlined under Jumper Options

Kits are not configured at factory.

P188
S100 Bus 8088 Processor Board

The P188 is an 8088 processor on a standard S100 board. The P188 will run in 3 modes, allowing maximum flexability in S100 systems of different configurations. The P188 emulates all necessary S100 bus signals. Numerous jumpers allow configurating the card to run different operating modes, as well as static and dynamic memory.

The 8088 processor is from four to six times more powerful than the 8080A. Providing 5 MHz processing speed, with an external bus of 8 bits, it has 16-bit internal architecture. Also, 8-bit and 16-bit signed and unsigned arithmetic in binary or decimal, including multiply and divide. The 8088 will address 1 megabyte of memory.

The 8088 is an 8086 with an 8-bit external data bus instead of a 16-bit bus. In applications that manipulate 8-bit quantities extensively, or that are execution-bound, the 8088 can approach to within 10% of the 8086's processing throughput. With pipelined architecture, allowing instructions to be prefetched during spare bus cycles, and internal 16-bit data path, and a compact instruction format, the 8088 realizes its high performance.

The P188 will operate in 3 modes:

1. As a stand-alone processor on the S100 bus
2. As a slave processor to a Z80, 8080 or other S100 processors
3. In a multi-processor mode with one or more additional processors on the bus

As a slave processor to a second processor card on the bus, control can be transferred via software commands. When the transfer command line is activated, the P188 will issue a HOLD command. Upon receipt of a HOLD ACK from the master processor, the P188 will take over the bus and start executing instructions at memory location FFFF0H. The P188 can transfer control back to the master processor by releasing the transfer control line.

It is necessary for the transfer control line to be driven by an I/O port external to the P188. It can be controlled from an external switch as well as an I/O port.

In systems where it is necessary to have 2 or more processors that can become masters, the P188 can be jumped to allow all interface lines to be removed from the bus. It is necessary for the other processors in the system to also be able to remove all lines from the bus. This can be accomplished on most existing processor boards with a slight modification. Thus, implementing a true multi-processor environment.

The bus interface of the P188 allows for 48 MA output current sink. Therefore, they will perform well in large systems with or without bus terminators. Also, all control inputs have an RC filter and Schmitt-trigger to improve noise margins.

A LED indicator on the P188 card is on when it is in control of the bus. Two prototype IC locations are provided on the card to help implement special requirements. A 26-pin connector is provided on top of the card to interface auxiliary control functions, such as the transfer command line.

Various software systems have been or are being developed for the 8086-8088 (the 8088 is fully software compatible with the 8086). Some are as follows:

CP/M-86
Digital Research
P.O. Box 579
Pacific Grove, California 93950
(408) 649-3896

Trans 86
Converts 8080/Z80 Code to 8086/88 code
SORCIM
133 Lawrence Expressway. Suite 418
Santa Clara, California 95051

BASIC-86
Xenix (Unix)
XMACRO-86 - Cross Assembler
Assembles 8086 code on any 8088-Z80 system compatible with CP/M
Microsoft
10800 N.E. Eighth, Suite 819
Bellevue, Washington 98004
(206) 455-8080

Books: The 8086 Primer, by Stephen P. Morse
Hayden Book Company, Inc.
Rochelle Park, New Jersey

The 8086 Book (includes the 8088)
Russell Rector - George Alexy
Osborne/McGraw-Hill
630 Bancroft Way
Berkeley, California 94710

The 8086 Family User's Manual
Intel Corporation
Literature Department
3065 Bowers Avenue
Santa Clara, California 95051

NOTE: Knowledge of the 8088's use and operation is beyond the scope of this manual. The above books will complement this manual and assist in trouble-shooting the P188.

P188 SPECIFICATIONS

CPU - 8088 with 5MHZ clock

Address Lines - 20 (1 megabyte addressing)

Data Lines - 8 in/8 out

CPU Internal - 16 bit internal architecture, 8-bit/16-bit signed and unsigned arithmetic in binary or decimal, including multiply and divide

Power Required - 8V unregulated at 0.9 amps

PC Card - Double sided, plated through holes, gold fingers solder mask both sides

IC Layout - 12 x 3 matrix with 2 spare sockets

Optional Connector - 26 pin flat cable at the top of card

Bus - S100, IEEE standard

Line Drivers - 8T97, sinking 48 ma.

Line Receivers - control lines have input filter with Schmitt-trigger receiver

Jumper Options - 22 to select operation mode and other options

LED Indicator - on when in 8088 mode

Transfer Command - via external I/O port, accessed through external 26 pin connector or spare S100 Bus line

Control Transfer - via external I/O port of external switch

Operating Modes - 3 stand-alone processor, slave processor and multi-processor

IC's Required - 30 and 2 5V regulators

Burn-in - assembled and tested units receive burn-in prior to shipping

Sockets - A & T unit and kit are supplied with sockets for every IC

Manual - assembly information, board checkout, jumper options, theory of operation, assembly print and schematic diagram

ASSEMBLY INSTRUCTIONS
and
PARTS LIST

ASSEMBLY DRAWING

While assembling the P188, refer to the P188 Assembly Drawing for part location. IC orientation is important; Pin 1 should be oriented so it is on the top left-hand corner, except for the three 74LS75's and the 8088. All part values and their reference number are shown on the assembly drawing.

SOLDERING TIPS

The P188 board comes with a solder mask to prevent unintended solder connections. It is still advisable when soldering to use care and avoid excessive solder build-up. Use 60/40 resin core solder. DO NOT USE ACID CORE SOLDER. Use a 15 to 25 Watt iron with a small tip. Heat the pad until the solder flows evenly. Overheating a pad can cause pad lift-off. If the resultant solder joint is not shiny, it may be a cold solder joint causing poor connection. Re-heat to obtain proper appearance. Keep the tip of the soldering iron clean by frequently wiping on a damp sponge.

COMPONENT SIDE

The component side of the board has the ACOM ELECTRONICS and P188 label. Also, the location references 1 through 12 across the top and A-B-C down the right side.

ASSEMBLY STEPS

1. Install the two regulators and heatskinks with the 6-32 screws. Solder the regulators in place. Install the 33 mf cap (C37) and the 3 22uf caps (C36, C35 and C34). Make sure the + lead of the capacitor is oriented as shown on the assembly drawing. Install the card in a S100 back plane and measure the power in Row "A" for +5V. Also, measure the power in Row "C" for +5V.
2. Install all the sockets (30 each)

Location	Device	No. of Pins
A6	8088	40
A3	8284	18
A12	74LS138	16
B8, B6, B5	74LS75	16
C3 thru C11	8T97	16
All the rest		14

Install the sockets so pin 1 is oriented as shown on assembly drawing. Install all sockets and hold to board by taping a piece of cardboard over sockets. Turn board over and solder sockets in place.

3. Install and solder the .047 mf decoupling capacitors in the locations marked DC inside a rectangle on the assembly print.
4. Make right angle bends in the leads of each resistor to match the .4 inch spacing of the resistor pads on the card. Install and solder each resistor in place. Use the assembly drawing as a guide so the correct value will be in each location.
5. Install and solder the 47 PF capacitors. They are shown on the assembly drawings in rectangles marked with an X.
6. Install and solder the 15 MHZ crystal. Leave enough lead length so that the crystal can be bent flat against the card. With the crystal in place, solder a wire in the two mounting holes and around the case of the crystal to hold the crystal in place.
7. Install and solder the LED in place. The LED should lay flat against the card.
8. Install and solder P2, the 26 pin header.
9. For jumper connections, refer to jumper option in this manual. Solder in jumpers to match the configuration you wish to operate in.

PARTS LIST P188

Integrated Circuits

Quantity	Number	Q #	Location Code
1	74LS02	2	A11
2	74LS04	3,10	A10, B11
1	74LS13	5	A8
3	74LS14	4, 12, 17	A9, B9, B2
1	7416	33	C2
1	74LS32	16	B3
1	7438	19	C12
4	74LS74	8, 9, 11, 18	A8, B12, B10, B1
3	74LS75	13, 14, 15	B8, B6, B4
1	74LS132	34	C1
1	74LS138	1	A12
9	8797	20 thru 32	C3 thru C11
1	D8088	6	A6
1	P8284	7	A3

Capacitors

Quantity	Number	Value
17	C1 thru C16 C38	.047MF Ceramic Disc
18	C17 thru C33 C39	47PF Ceramic Disc
3	C34 thru C36	22MF 6 V Dipped Tantalum
1	C37	33MF 25V Dipped Tantalum

Resistors

17	R1 thru R17	1.2K ohms ¼W 5% Carbon
17	R18 thru R33 R38	150 ohms ¼W 5% Carbon
1	R34	100 ohms ¼W 5% Carbon
3	R36 R35 R37	4.7K ohms ¼W 5% Carbon

LED

1	XC111R	.190 Dia

Crystals

15,000 MEG.HZ

Connector

1	Jumper Header	Right-Angle 26 Pin

Diode

1	D1	IN4148

Voltage Regulators

2	LM340T-5 (7805)	5-Volt Positive Regulator
2		Heat Sink

Sockets

30 — 14 PIN-15 ea. 16 PIN-13 ea. 18 PIN-1 ea. 40 PIN-1 ea.

JUMPER OPTIONS

Each jumper on the P188 card is designated on the card by a letter, A,B,C, etc. A 26 pin option interface connector is provided on top of the card. Also, a 2-chip prototype area is provided on the top left-hand corner of the card. All jumper connecting pads are square. The jumper pad's location is shown on the assembly drawing. All letter designators appear on the card. Each group of pads for one letter designator are numbered 1,2,3, etc. The numbers do not appear on the card, but are determined by referring to the assembly drawing.

DBIN SYNC STVAL PWR

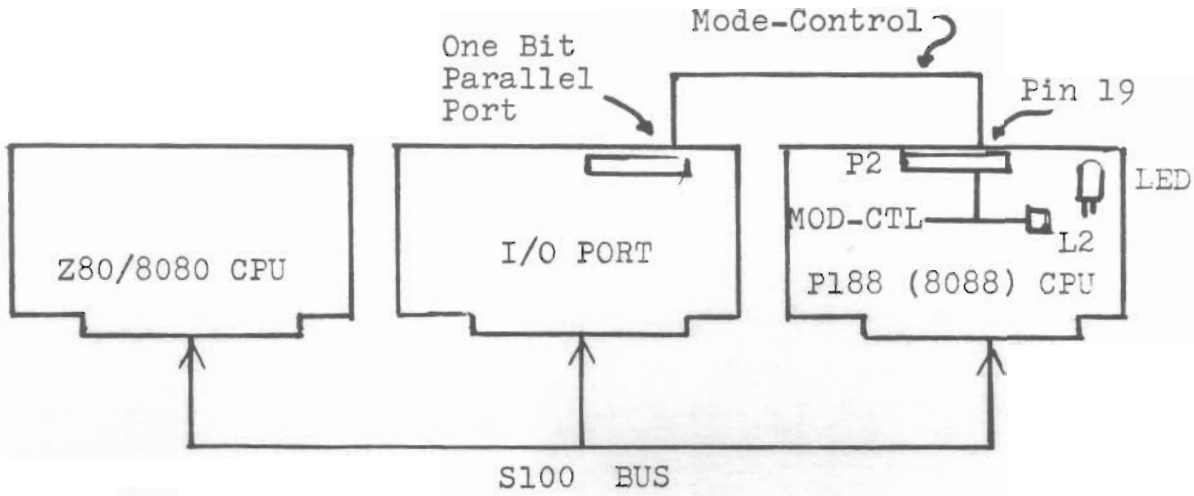
Jumper	Functional Description
A	Allows the connection of XRDY (pin 3) on PIN-21 of P2.
B	Allows PSYNC to equal ALE (8088) or to be delayed by one 8088 clock cycle.
C	Allows the trailing edge of M1 to be at the middle of T3 or the middle of T4.
D	Connected to P2 PIN 1
E	Connects the 8088 reset to the slave processor mode flip-flop.
F	Determines the signal that will generate *STVAL. The 3 signals are PS, *CLK or a combination of both.
G	Allows the clock and reset signals, CLOCK, Ø, *STVAL, *POC and *SLAVE CLR, bo be permantently enabled, permanently off or disabled by control disabled (*CDSB).
H	Allows the 4 disabled gates to be controlled by the mode control flip-flops
I	Not used.
J	Allows connection of PHLDA (pin 26) to the 8088 HLDA function. This is left open when the 8088 is running as a slave processor.
K	Allows connection of PINTE (pin 28) to the interrupt status flip-flop, which reflects the status of the 8088's interrup enabled flag bit.
L1	Allows connection to the input of a spare receiver.
L2	Allows for an external connection of the mode control flip-flop input.
M	Allows the CLOCK function, pin 49, to be connected with the P-CK function. Note: With a 15 MHZ Xtal, P-CK will be 2.5 MHZ or ½ of the 8088 clk (5MHZ). Some S100 boards require the frequency to be 2 MHZ. The Xtal would need to be 12 MHZ or M jumper is left open and 2 MHZ supplied from a different source.

N	Allows connecting the status drivers disabling function to the status disable function or the control disable function.
O	Not used.
P	Controls the M WRT and PHLDA driver. Allowing connection to ground (always enabled), status or command enable.
Q	Not used.
R	Connections for spare S100 pins 65 and 66. Also, enables selection of S100 pin 12 (NMI) or pin 13 (PWRFAIL) to be connected to 8088's NMI88 pin 17. (NMI = nonmasked interrup)
S	Allows M WRT function to be disconnected from the S100 bus. This is for units with a front panel.
T	Allows disconnection of the HOLD function of the 8088 from the S100 bus. This is necessary when the P188 is running as a slave processor.
U	These 4 jumpers connect the 4 disable gates to the S100 bus. These are connected when the P188 is used as the primary processor.
V	Allows grounding of the TEST input to the 8088.
W	Not used.
X	Oscillator output of the 8284. Will have a frequency equal to crystal frequency.
Y	Allows grounding of the F/C and C SYNC signal on the 8284. C sync is normally grounded unless an external event is used to synchronize the 8088 clock. When F/C is grounded, the 8088 clock is generated by the crystal. When F/C is high, the clock for the 8088 source is P2 pin 3.
Z	Allows the output of the spare receiver at A9 to be connected to P2 pin 11.

* (i.e., *CDSB) indicates a low active signal.

JUMPER CONNECTIONS

Switching from Z80 to 8088 Under Program Control

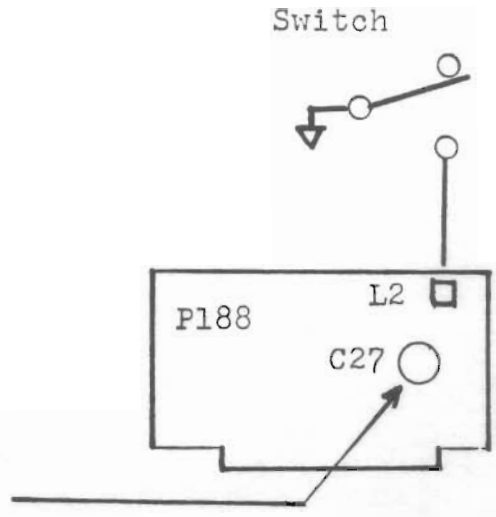


MODE CONTROL LINE

Low - 8088 Enabled, LED on, Z80 in HOLD mode

Hi - 8088 Reset, LED off, Z80 Enabled

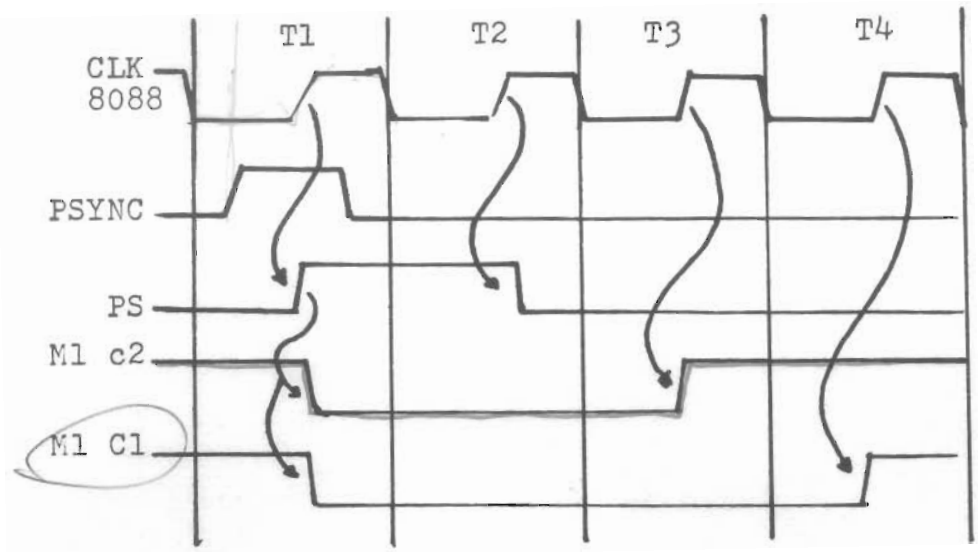
FOR TRANSFER WITH AN EXTERNAL SWITCH

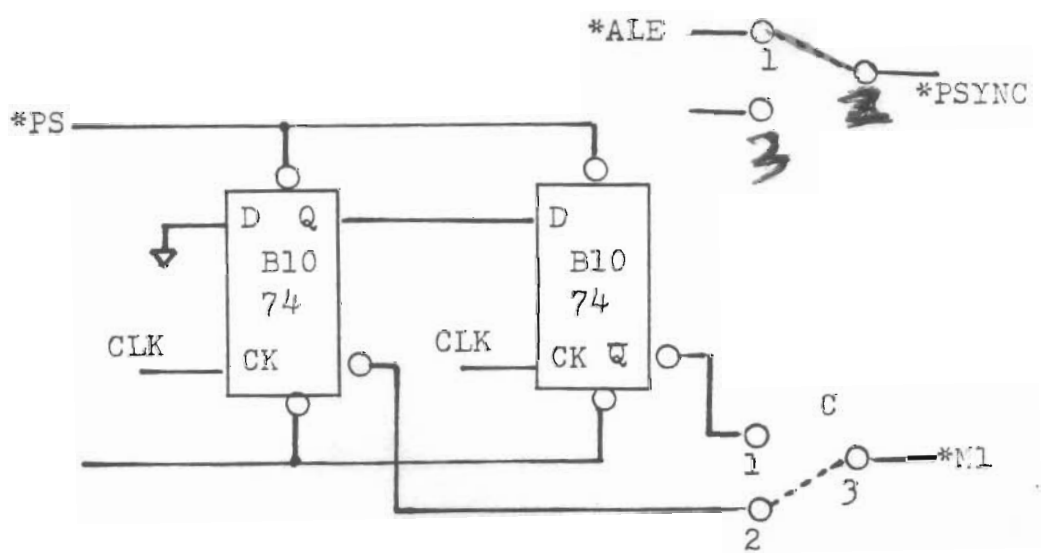


Note:
To eliminate switch bounce, replace C27 (47pf) cap. with a 22mf 6V cap.

JUMPER CONNECTIONS

M1 Operation for Dynamic Memory

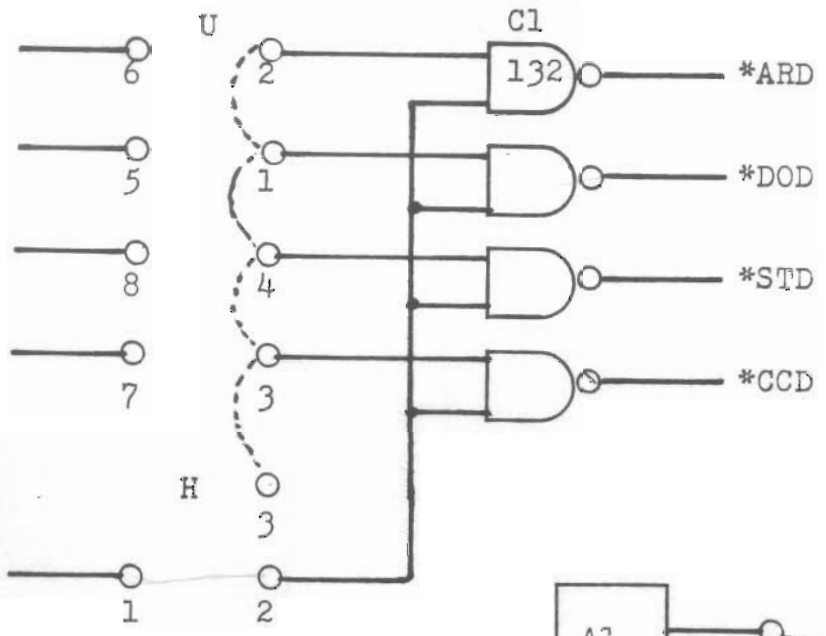


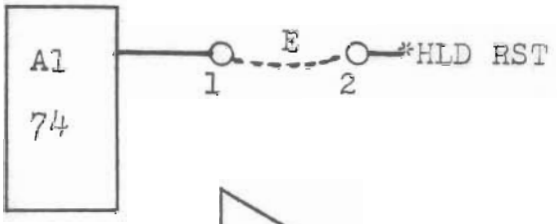


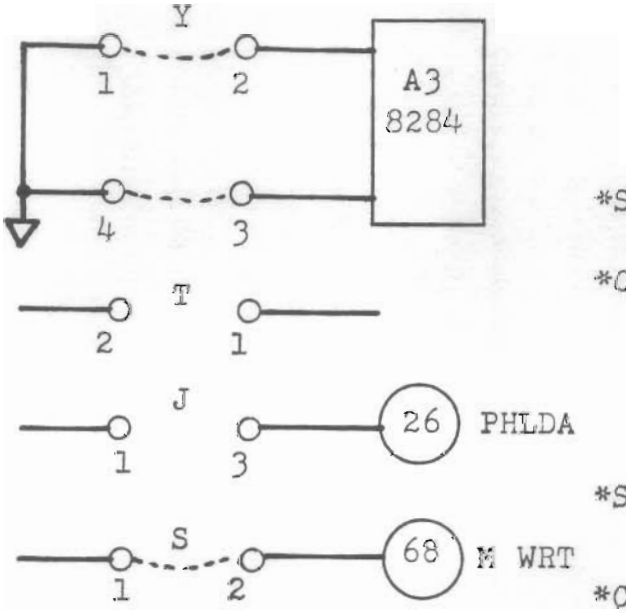
*SM1 is only active during an opcode fetch cycle.

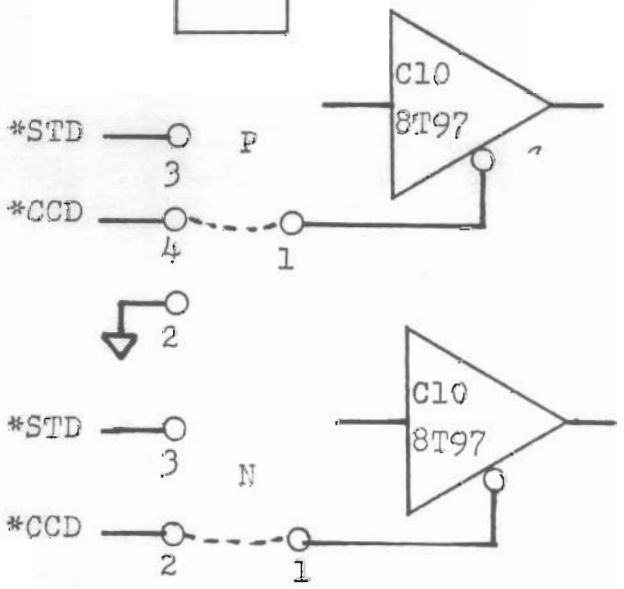
JUMPER CONNECTIONS

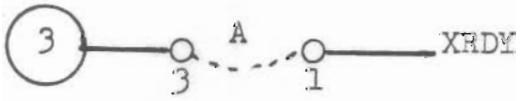
P188 as a Slave Processor



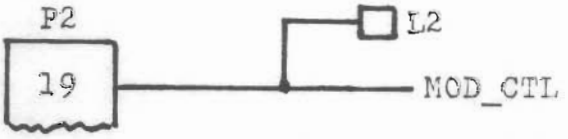






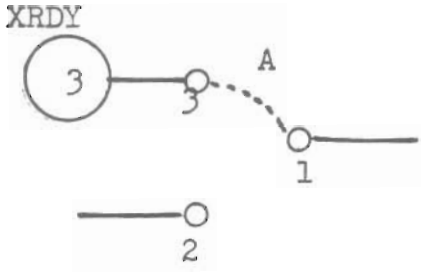


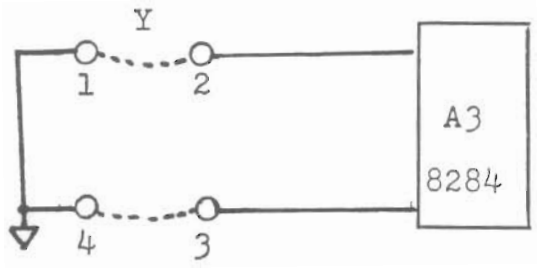
S is open if unit has a front panel.

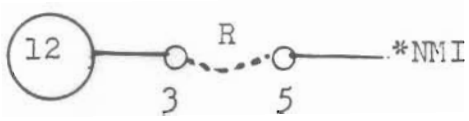


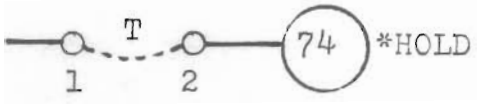
JUMPER CONNECTIONS

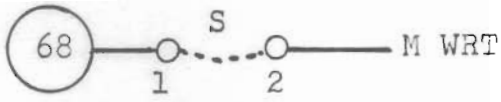
P188 as a Stand-alone Processor

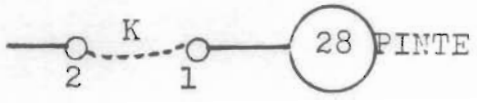




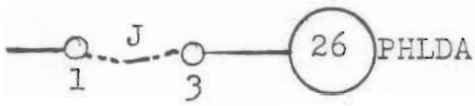


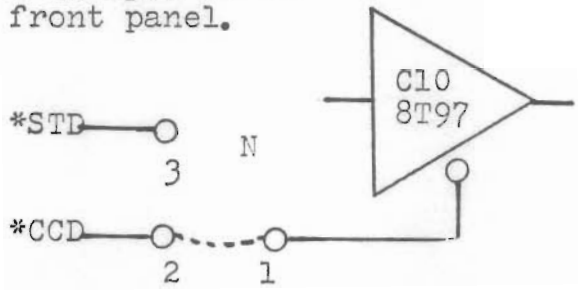


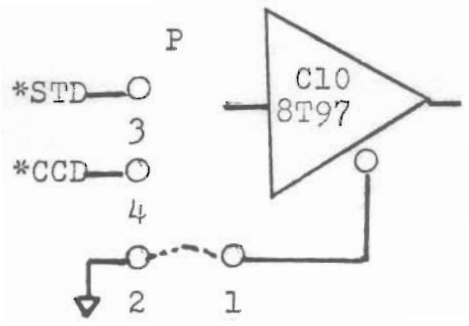


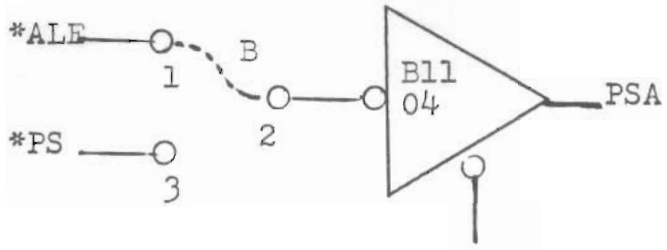


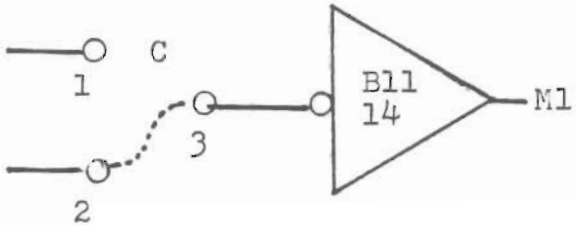
S is open if unit has a front panel.





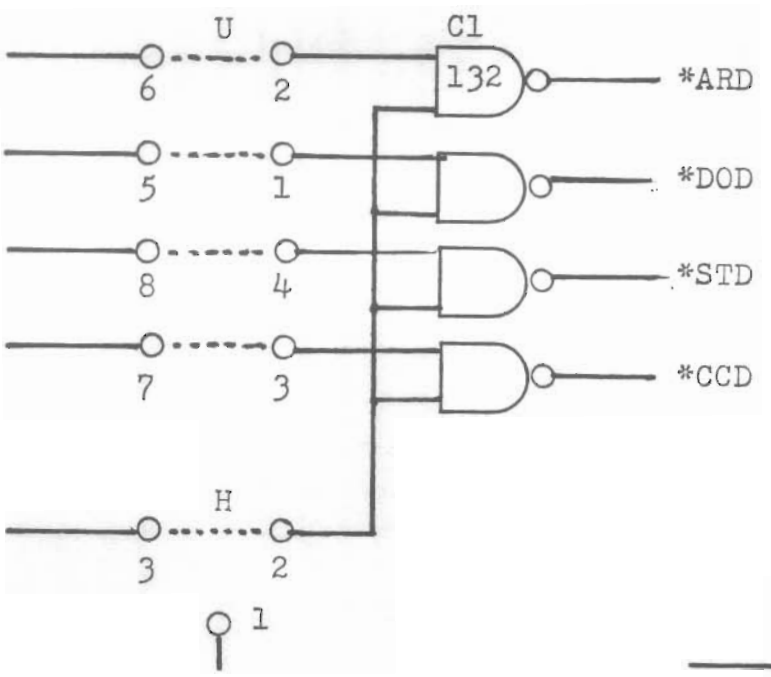


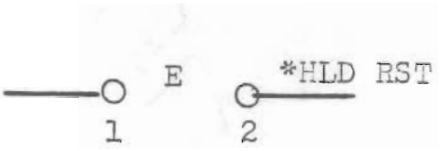


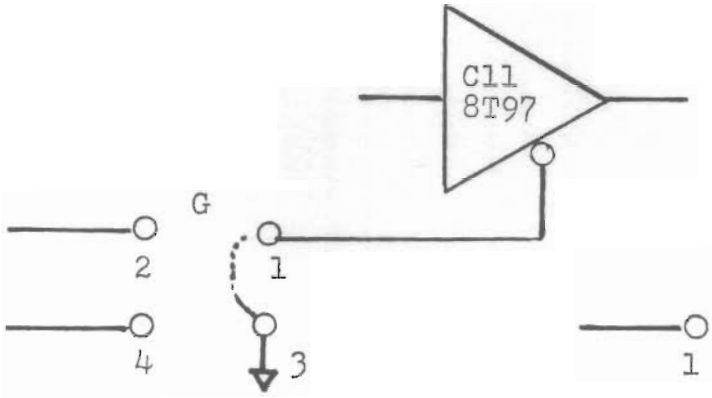


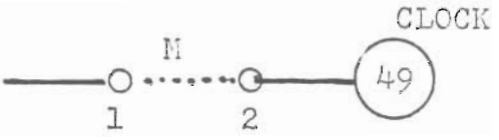
JUMPER CONNECTIONS

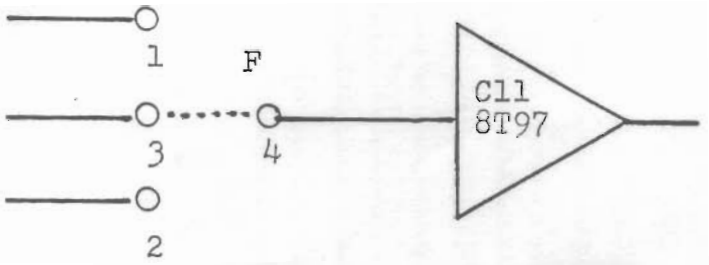
P188 as a Stand-alone Processor Con.





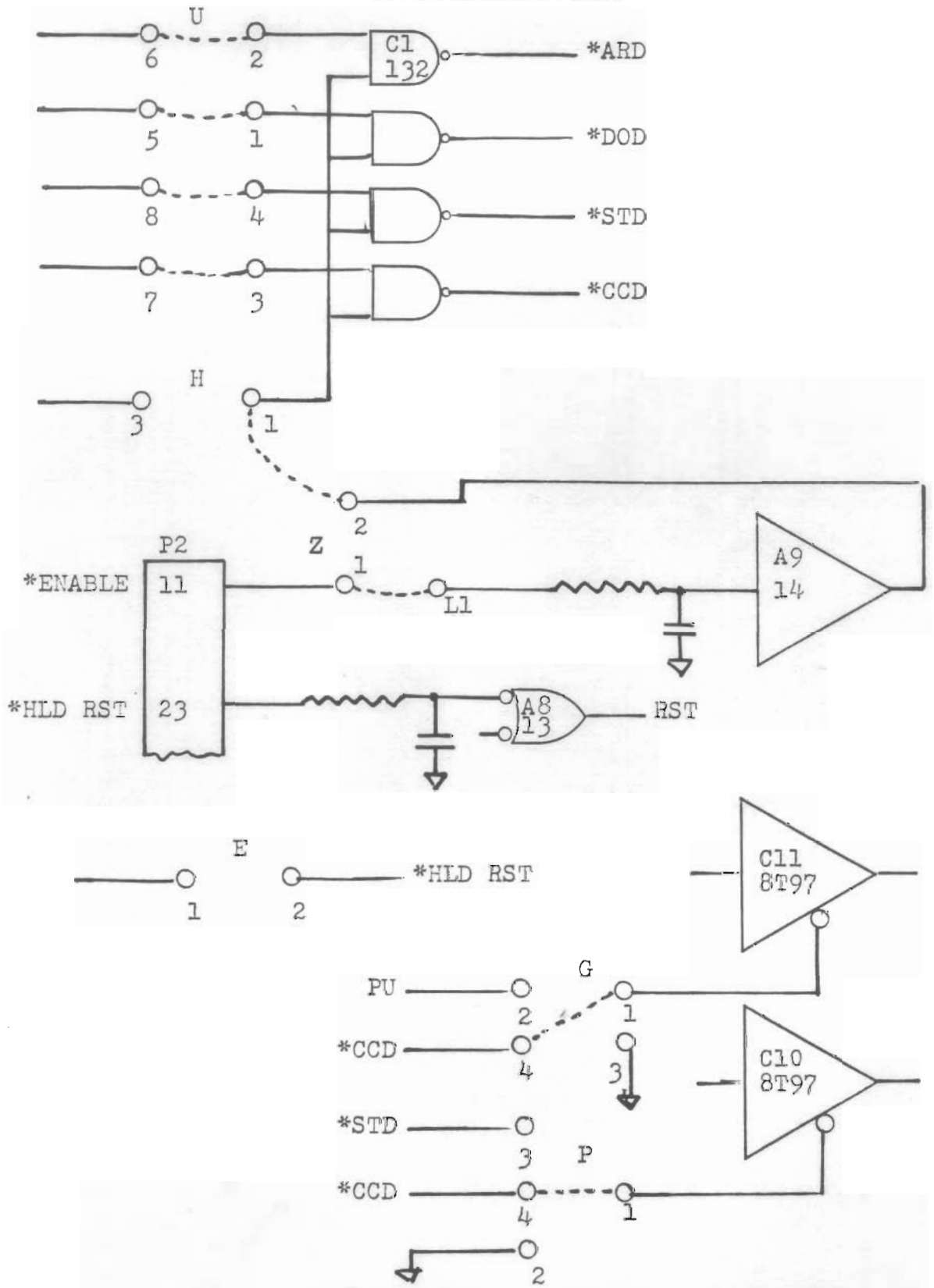






JUMPER CONNECTIONS

Shared Processor Mode



Remaining jumpers as shown for stand-alone processor.

THEORY OF OPERATION

CONTROL

The main function of the P188 is to provide interface between the S100 Bus and the 8088 microprocessor.

Sheet 1 of the schematic diagram covers the control interface between the 8088 and the S100 Bus. Also, shown on sheet 1 of the schematic diagram is the interface between the 8088 and P2, which is located on top of the card. P2 is used for external control and clocking of the card. All control inputs are filtered by a 150 ohm resistor and 47PF capacitor prior to being applied to a 74LS14 Schmitt-trigger. This combination provides excellent noise immunity of bus noise.

CLOCK CHIP

The 8284 is the clock generator for the 8088. A 15 MHZ crystal controlled oscillator is divided by 3 to provide a 5 MHZ clock for the 8088. This clock is labled CLK 88. The PCLK output of the 8284 is ½ the frequency of CLK 88. PCLK can be applied to pin 49 of the bus by using jumper M. For PCLK to be 2 MHZ, as required by some S100 BUS cards, the 15 MHZ crystal must be replaced by a 12 MHZ unit. This give a CLK 88 of 4 MHZ and a PCLK of 2 MHZ. The CLK 88 is applied to pin 24 of the bus through an 8T97 driver.

EXTERNAL CLOCK

For running the 8088 from an external clock, the F/*C input to the 8284 is held high with the external clock applied to pin 3 of P2. For synchronization with an external event, C SYNC is held high, which holds the divide by 3 counters reset until C SYNC is low. For normal operation, jumper Y 1,2 and Y 3,4 are installed.

READY

The 9294 also supplies the READY and RESET signals to the 8088. When the RDY 1 input receives an active high level, it is synchronized with the 8088 clock and applied to the READY input of the 8088. Ready is derived from A8 which requires three inputs to be high to allow the 8088 to run. With READY low, the 8088 will idle in wait cycles at the 8088 T3 clock cycle. Pin 13 of P2

must be high or the 8088 will be in a wait state. Also, pin 72 of the bus (RDY) must be high. Pin 3 of the bus (XRDY) or pin 21 of P2 can be selected via jumper A to perform the READY function.

RESET

Reset is applied to the 8284 and then to the 8088 from the inputs of gate A8. If pin 23 of P2 is held low, the 8088 will be held resent. Also, pin 75 of the bus going low will hold the 8088 reset. A power on reset circuit consisting of a 1.2K resistor, 22 mf capacitor and diode, will cause the 8088 to reset when power is applied. The third input to the reset side of A8 is *HLD RST. This signal comes from the mode control circuit shown on sheet 3 of the schematic diagram. When the P188 is jumpered to run as a slave processor, the 8088 is held reset by the *HLD RST line until a change mode command is received. The *HLD RST line is raised high allowing the 8088 to run. When the 8088 starts executing instructions after a reset, the first addressed accessed is FFFFOH.

TEST PIN

When the 8088 encounters a wait instruction, it will wait until the *TEST pin (23) is brought active low. Therefore, the 8088 can be synchronized with external events. Access to the * TEST pin of the 8088 is through P2 pin 9 or jumper V.

SPARE RECEIVER

Test point L1 supplies a connection point to the spare receiver input. The output of the receiver is available at Z2, with Z1 connected to pin 11 of P2. This option extends the flexibility of the P188.

HOLD

The *HOLD control line on the bus (pin 74) is applied to the 8088 HOLD input when jumper T is in place. When HOLD is active high, the 8088 will suspend operation and issues a PHLDA (hold acknowledge) which is applied to the bus on pin 26 when jumper J is in place.

The HOLD function is used by an external device to gain control of the bus. To disable the bus drivers, the external device must also activate the 4-bus

disable lines. This required the 4 U jumpers to be in place. Thus, with the I, J and 4U jumpers in place, the P188 is configurated to operate as a master bus controller. For detailed operation of the disabling lines, see the mode control section.

STATUS DECODE

Status is decoded using A12 (74LS138). Using pin 34 of the 8088 (*SSO) and IOM with DT/R, the 84LS138 will decode the type of bus cycle. When all three lines are a 1 level, active high, a HALT is indicated. This is applied through a bus driver to pin 48 of the bus (SHALT). This line will remain active as long as the 8088 is halted.

When all three lines are 0, active low, the 8088 is executing an op code fetch. The *CODE line of A12 will go active low causing the clear on flip-flop B10 to be removed. This allows *PS and CLK to issue a pulse on the output of B10. Jumper C is used to select the length of the pulse, M1. The M1 pulse is applied to the bus driver for pin 44 (SM1). This signals the memory cards that an op-code fetch is in progress and is used by dynamic memory to cause a refresh cycle. Other status decodes are available on the pins A12 as specified in the following table:

A12 Pin	IO/*M	DT/*R	*SSO	Function
7	1	1	1	HALT
9	1	1	0	I/O WRITE
10	1	0	1	I/O READ
11	1	0	0	INT ACK
12	0	1	1	NO.OP
13	0	1	0	MEM WRITE
14	0	0	1	MEM READ
15	0	0	0	CODE SEG ACCESS

INTERRUPT FACILITIES

The 8088 has 2 interrupt imputs and 1 output. The NMI88 input, pin 17, is the highest priority interrupt. The activation of this pin causes a type 2 interrupt, vectoring the 8088 to the address specified for NMI (non-maskable interrupt). NMI must be high for at least 2 clock cycles to guarantee recognition. Jumper R allows the selection of bus pins 12 (XNMI) or 13 (*PWRFAIL) to be connected to the NMI88 pin. Power fail is a typical use of the non-maskable interrupt.

The INTR input, pin 18, is for requesting hardware maskable interrupts. These interrupts are masked by the IF bit (Interrupt flag) of the program status word. The INTR is sampled during the last clock cycle of each instruction cycle. The INTR input is connected to pin 73 of the bus (*INT) via a bus receiver. The INTR must be held active until the 8088 returns an interrupt acknowledge.

The acknowledge is returned via *INTA, pin 24, two interrupt acknowledge pulses will be transmitted during an interrupt acknowledge sequence. The interrupt number, type vector, is transferred to the 8088 on the data bus during the second *INTA bus cycle.

READ WRITE CONTROL

Three 8088 lines are involved in read and write control. The IO/M, pin 28 of the 8088, determines if the read or write is for IO or memory. Pin 29 is the write output of the 8088 and pin 32 is the read output of the 8088. Gate A11 decodes these three signals to match the required S100 bus signals. The SOUT and SINP lines are driven for IO read or write, whereas SMEMR and MWRT are driven for memory read and write. Jumper S allows for disconnecting MWRT, pin 68, this is required in systems with a front panel. The S100 *SWO is driven directly from the *WR88 line.

PSYNC

The S100 bus singal, PSYNC, indicates the start of a new bus cycle. The ALE output of the 8088 indicates the start of a new bus cycle with the trailing edge of ALE indicating the address is latched on the P188 and the address is stable on the bus. Jumper B allows for PSYNC to be derived from ALE or a delayed ALE, re-clocked by the 8088 clock.

ADDRESS SIGNALS

The 8088 supplies 20 address lines to the S100 bus. This allows addressing of 1 megabyte of memory. The lower 8 bits of the address are multiplexed with the data. Therefore, it is latched with the two 4-bit latches, B4 a B7. The next higher 8 bits of memory are not latched because they are not multiplex with data. They are applied directly to the bus through the drivers. The most significant 4 bits, A16 to A19 are latched by B8 since the 8088 multiplexes these lines with status data. This status data is not used by the P188 since it decodes its status as covered under the status decode section.

DATA BUS

Two 8-bit data buses, DATA IN and DATA OUT are interfaced to the bidirectional data bus of the 8088 with 8T97 drivers (C3, C4 and C5). These drivers are enabled by gate B3 using the *DT, data transmit, and *DEN, data enabled, signals from the 8088. Also, the B3 Decode for enabling DATA IN is used to generate the control signal PDBIN.

CLOCK SIGNALS & POC

The clock signals for the S100 bus are applied by the bus through driver C11. Pin 49 (CLOCK) can be derived from the P-CK output of the 8284, which is ½ the frequency of the 8088 clock. The 8088 clock is 5 MHZ with a 15 MHZ crystal. Jumper M allows disconnecting this clock so a different card on the bus can drive this line. The S100 bus specifications requires this line to be 2 MHZ.

The clock on pin 24 of the bus is the same as CLK 88, that is a 5 MHZ clock when using a 15 MHZ crystal. The clock on pin 25 can be derived from 3 sources using jumper F. It can be *CLK, which is the same as *CLK88, the PS flip-flop or a combination of both using gate C12.

MODE CONTROL

The grant control circuit, located on sheet 3 of the schematic, enables the P188 to run 3 modes. When the P188 is the primary processor on the bus, it is necessary for the line drivers to be disabled when a slave device uses the bus. Four lines are used to disable the P188-S100 lines. The are *ADSB (address disable), *DODSB (data out disable), *SDSB (status disable) and *CDSB (control disable).

Stand Alone Processor - When the P188 is functioning as a stand-alone processor, the four U jumpers are connected allowing gate C1 to pass the inverted disable signal onto the appropriate line drivers. For this application, jumper H and E will be left open.

Jumper T (HOLD) and jumper J (HOLD ACK) will be connected. Therefore, when an external device takes control of the bus, the P188 will respond in the standard way for S100 bus processors. Jumpers P and N must be connected to a status or control enable function. Normally, the clock and reset lines are not removed from the bus, thus jumper G allows for the signals to be always on the bus by grounding the enable function.

Slave Processor - When the P188 is used as a slave to a 2nd processor on the bus, the jumpers mentioned above are configurated differently. The P188 must drive the disable lines. This it does through IC C2 in a sequence controlled by the 3 flip-flops B1a, B1b and A1. To effect a transfer of bus control, the *MOD-CTL line is lowered, which will cause flip-flop B1a to set on the next bus clock. This will cause the bus HOLD signal line to be activated when the master bus processor responds with a HOLDA (hold acknowledge), signaling the P188 that it can take the bus. The PHLDA will set flip-flop B1b. With jumper H in place, and the U jumpers open, the P188 bus drivers will be enabled. Also, at this time the S100 bus disable lines will be activated, disabling the drivers in the master processor. The LED, indicating the P188 is in control, will be turned on.

The control disable line will not be activated at this time. It will be activated on the next bus clock cycle. This will overlap the control lines enabling and disabling in the two processors to prevent false control signals appearing on the bus. Flip-flop A1 will be set to complete the cycle. Jumper E will be connected so that the 8088 is held reset until the P188 has control of the bus. When *HLD RST goes high, the 8088 will start executing at location FFFF0H. Jumper G would be connected to a PU (pull up) to turn off the clock and reset drivers of the P188 since the master processor on the bus will most likely have clock and reset lines permanently connected.

Multi-Processor - If more than one master processor is to share the bus and a device, such as a disc controller, should be able to do DMA accesses, regardless of which processor is in control of the bus, then a multi-processor configuration must be employed. To implement this mode, the selection flip-flops (A1 and B1) are not used. The U jumpers, as well as the T and J jumpers are connected as they would be when the P188 is the only processor on the bus. Jumper L1 is connected to P2 pin 11 via Z1. Jumper Z2 and H2 are connected. This allows an external signal to enable the drivers on the P188. Also, an external signal can start the P188 through P2 pin 23. With this setup, the P188 will respond normally when a hold is requested, but still be disconnected from the bus when a 2nd processor is to be applied to the bus. An external control circuit is required to pass control from one processor to the next.

VOLTAGE REGULATIONS

Two 7805, 5 volt regulators, with heat sinks are provided on the card. These convert the +8 volts of the bus to 5 volts for use on the card. Each regulator drives a separate power bus, dividing the load evenly.

APPENDIX 1

S100 Bus Pin List IEEE STD.

Pin No.	Signal	P188 Use	Pin No.	Signal	P188 Use
1	+8 volts	X	51	+8 volts	X
2	+16 volts		52	-16 volts	
3	XRDY H	X	53	GND	
4	VIO L		54	SLAVE CLR	X
5	VI1		55	DMAO	
6	VI2		56	DMA1	
7	VI3		57	DMAZ	
8	VI4		58	SXTRQ	
9	VI5		59	A19	
10	VI6		60	SIXTN	
11	VI7		61	A20	
12	MMI	X	62	A21	
13	PWRFAIL	X	63	A22	
14	DMA3		64	A23	
15	A18	X	65	Not used	
16	A16	X	66	Not used	
17	A17	X	67	PHANTOM	
18	SDSB	X	68	MWRT	X
19	CDSB	X	69	Not used	
20	GND	X	70	GND	X
21	Not used		71	Not used	
22	ADSB	X	72	Not used	
23	DODSB	X	73	INT	X
24	Ø	X	74	HOLD	X
25	PSTVAL	X	75	RESET	X
26	PHLDA	X	76	PSYNC	X
27	Not used	disconnected used for PWAIT	77	PWR	X
28	Not used		78	PDBIN	X
29	A5	X	79	AO	X
30	A4	X	80	A1	X
31	A3	X	81	A2	X
32	A15	X	82	A6	X
33	A12	X	83	A7	X
34	A9	X	84	A8	X
35	DO1	X	85	A13	X
36	DOO	X	86	A14	X
37	A10	X	87	A11	X
38	DO4	X	88	DO2	X
39	DO5	X	89	DO3	X
40	DO6	X	90	DO7	X
41	DI2	X	91	DI4	X
42	DI3	X	92	DI5	X
43	DI7	X	93	DI6	X
44	SM1	X	94	DI1	X
45	SOUT	X	95	DIO	X
46	SINP	X	96	SINTA	X
47	SMEMR	X	97	SWO	X
48	SHLTA	X	98	ERROR	
49	CLOCK	X	99	POC	X
50	GND	X	100	GND	X

APPENDIX 2

P188 Test Program

This program will transfer control, back and forth, between the 8088 processor and the Z80/8080 processor. This will cause the LED on the P188 to blink on and off.

Z80/8080 Section

```
Location          Code
0200    Start     01 F0 F4      LXI B,F4F0      ;set up for delay
0203    Loop 1    0B 78 FE      DCX B           ; do delay
0204              78            MOV A,B
0205              FE 00         CPI 00          ;B equal 0 ?
0207              C2 03 02      JNZ Loop 1      ;no loop again
020A              79            MOV A,C
020B              FE            CPI 00          ;C equal 0 ?
020D              C2 03 02      JNZ Loop 1      ;no loop again
0210              3E 01         MVI A,01        ;set up A
0212              D3 xx         OUT xx          ;set up transfer F/F
```

:Set address xx to match the address of the output port that is connected to the transfer flip-flop (MOD-CTL) on the P188.

```
0214              00            NOP
0215              C3 00 02      JMP 0200        ;return to start
```

:When transfer F/F on the P188, is set, the Z80/8088 processor will be placed on hold until the 8088 releases the bus allowing the Z80/8080 to execute the jump at 0215.

APPENDIX 2 (Cont'd)

P188 Test Program

8088 Section

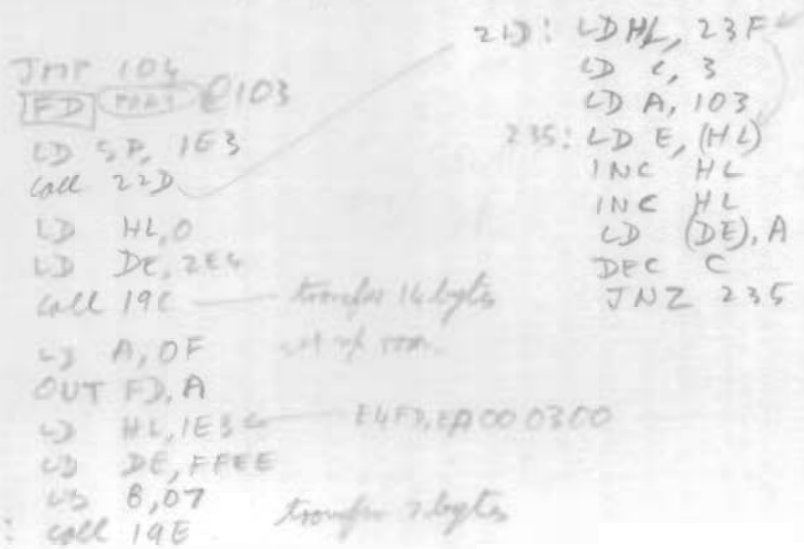
The 8088 will start executing at FFFFOH. At this location, a jump to the start of the 8088 program. In this case, it is location 0100H.

Location	Code	
FFF0	EA 00 01 00 00	JMP 0100,0000

:Jump direct intersegment - on reset, the code segment register is set to FFFFH. This jump command sets it to 0000H. The offset to the PC, which is set to 0000H on reset, is 0100H.

```
0100            B9 F8 F0    MOV i, CX       ;load CX delay value
0103    Loop    49          DEC CX
0104            75FD        JNZ Loop        ;loop again if not 0
0106            B0 00       MOV i, AL       ;set acc. to 0
0108            E6 xx       OUT xx          ;reset transfer flip-flop
```

:Set address xx to match the address of the output port that is connected to the transfer flip-flop (MOD-CTL) on the P188.

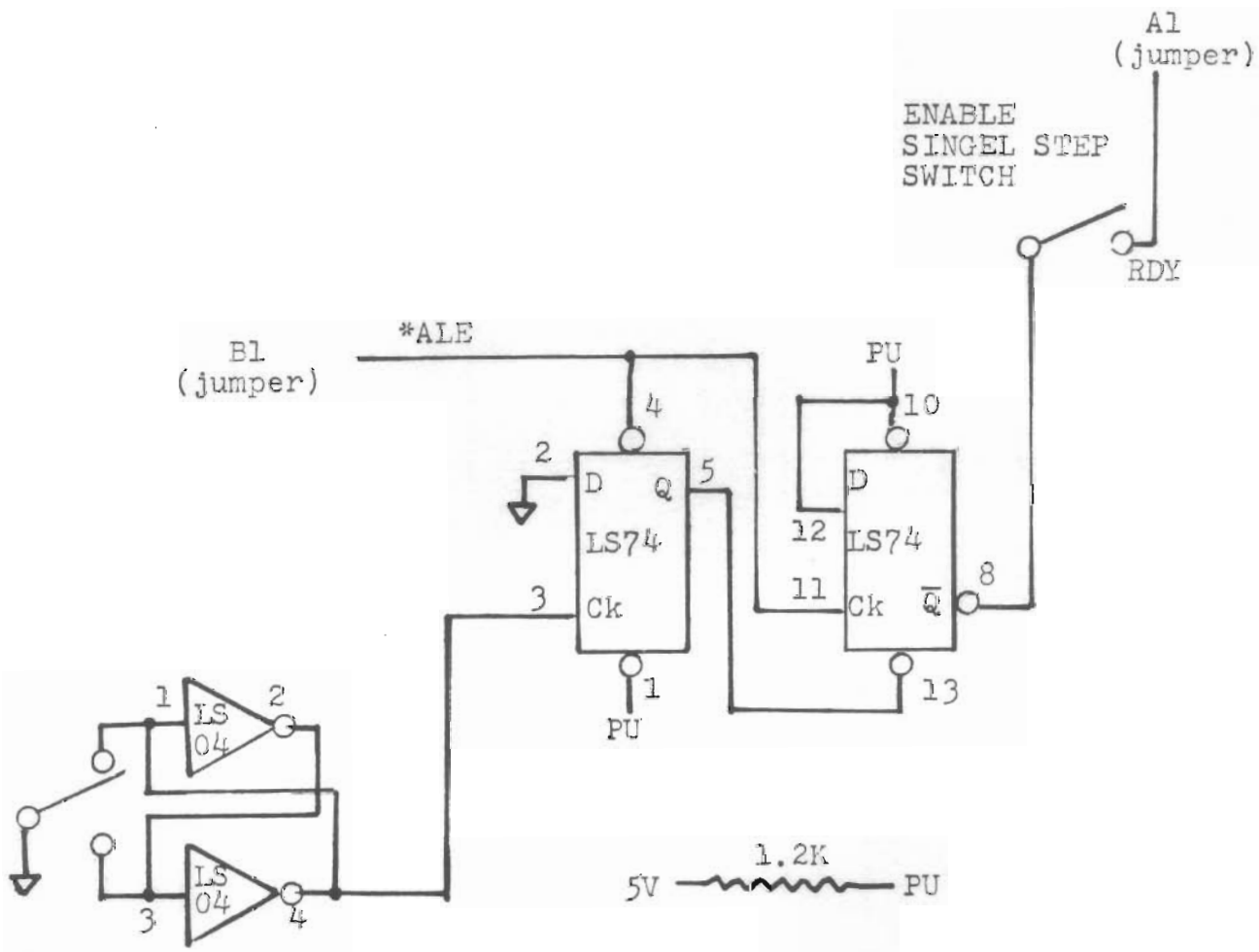


APPENDIX 3

Single Step Mode

The following hardware can be added to the P188 prototyping area so when installed in a S100 back plane with a front panel, it can run in signal step mode.

It must be remembered that the 8088 has a BIU that prefetches instructions and no data lights will be displayed because there is no data jumper provision for a front panel on the P188.



LIMITED WARRANTY

ACOM ELECTRONICS warrants its products to be free from defects in material and/or workmanship for a period of 90 days for kits and bare boards, and one (1) year for factory assembled boards from date of purchase.

In the event of a malfunction or other indication of failure attributable directly to faulty workmanship and/or material, ACOM ELECTRONICS will repair the defect at no cost to the purchaser. This warranty does not extend to malfunctions or defects resulting from improper use or assembly by purchaser.

This warranty does not cover transportation cost to Acom Electronics. Return the defective product to:

Acom Electronics
Warranty Department
4151 Middlefield Road
Palo Alto, CA 94303

This warranty applies only ot the original purchaser.

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This warranty is made in lieu of all other warranties, expressed or implied, and is limited to the repair or replacement of the product. No warranty, expressed or implied, is extended concerning the completeness, correctness, or suitability of the Acom Electronics equipment for any particular application. There are no warranties which extend beyond those expressly stated herein.

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ACOM ELECTRONICS will repair any of its products at a rate of $25.00 per hour. Send defected unit to Acom Electronics, Repair Department, post-paid. Include a description of the problem and any time limit you wish to place on repair. Acom will return the unit within 30-days after receipt. You will be billed for repair cost and return shipping.

ACOM ELECTRONICS------APPLICATION NOTE--P188-1

This application note describes how to jumper the P188 board for improved performance when transferring from 8088 to Z80 control when the system memory is dynamic memory.

Figure 1 shows the change to the SOUT driver input (IC location C3) to delay the application of a SOUT pulse to the S100 BUS during a 8088 I/O write cycle.

This is required because the 8088 write pulse can preceed data by 100NS in a worst case situation. A 120NS delay is provided by the circuit of Figure 1.

To implement the change of Figure 1, the trace connecting A11 pin 1 and C3 pin 12 is cut. This trace can be found on top of the card connecting to pin 1 and running past decoupling capacitor C2. A11-1 and C3-12 are reconnected using the circuitry shown in Figure 1. The resistors R19 and C19, connecting to L1 are replaced with a 330 OHM resistor and 330 PF capacitor. Flip-flop A1 will allow a delay for turn-on of SOUT with the turn-off of SOUT occuring when A11-1 goes low.

Two changes are made to the transfer control circuit on sheet 3 of the schematic diagram. This is shown in Figure 2. First the jumpers for U and H are changed. U-1, 2 and 4 are connected to H-1. Thus, when flip-flop B1-B is set or reset all control is transferred except for the control lines. U-3 is connected to B2-10, the PHLDA signal. This insures that the control lines are both on for apx 50NS on transfer to 8088 control and transfer from 8088 control.

Second, the trace from A1-pin 13 is cut and A1 pin 13 is connected to A1-pin 12. This causes the 8088 processor to receive a halt during the current SOUT cycle, preventing further 8088 control commands from appearing on the bus.

To locate the trace connected to A1-13, hold the card with the component side up. The A1-13 trace runs from the thru hole to the left of the E jumper up under the socket for A1. Cut the trace at the thru hole, leaving the trace from the thru hole down intact.

For this modification to function properly, the I/O part controlling the transfer control line (MOD-CTL) must be activated on the leading edge of the SOUT pulse.

This change has run in ACOM's lab with a test that transferred control once every second for several hundred hours without one transfer failure. The test was done with a dynamic RAM and a 4MHZ Z80.

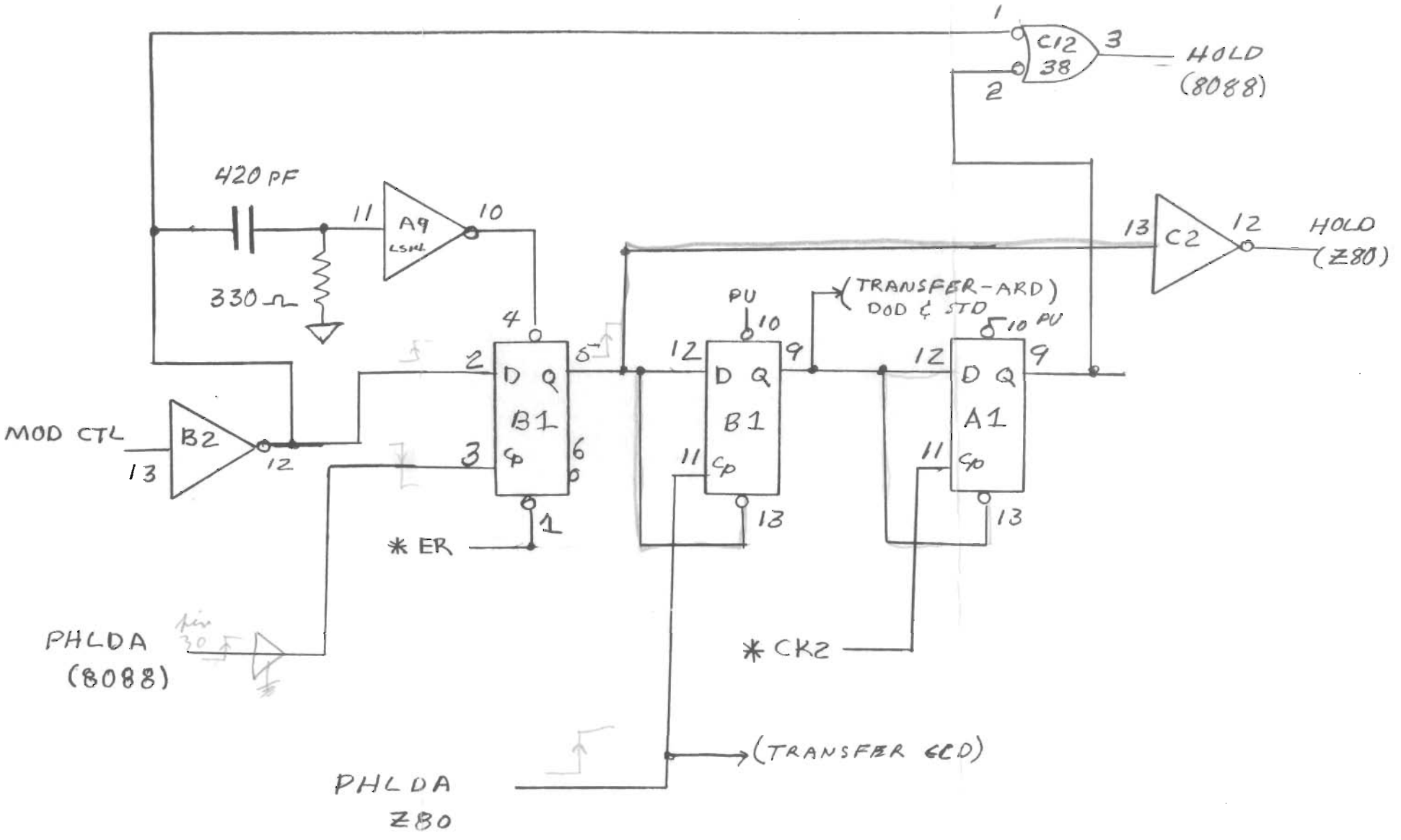
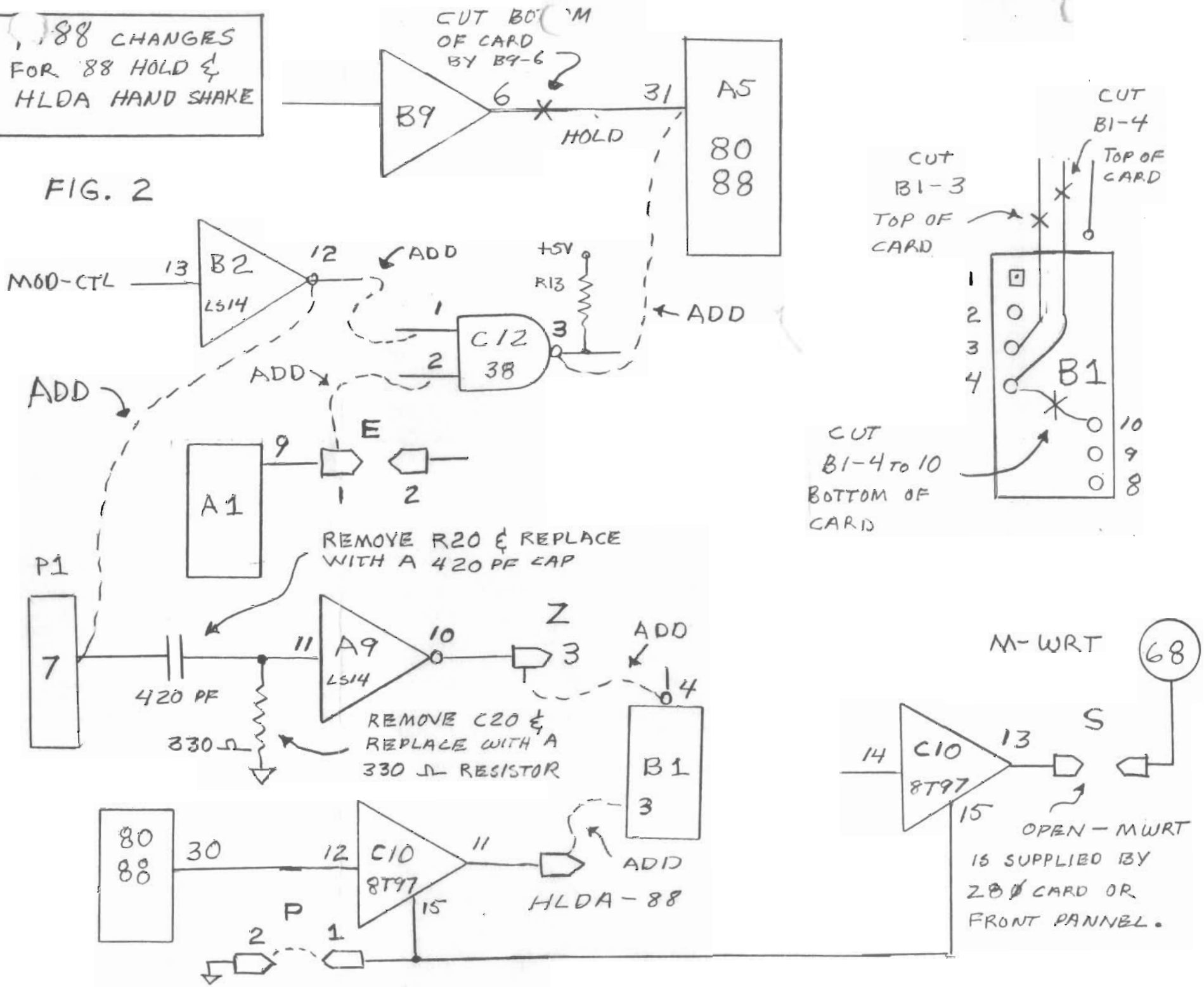


FIG 1

P188 8088 HOLD & HOLD ACK. HAND SHAKE

,188 CHANGES FOR 88 HOLD & HLDA HAND SHAKE

FIG. 2



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ACOM ELECTRONICS ---------- APPLICATION NOTE P188-3

This application note describes how to jumper the P188 board so that when you transfer from Z80/8080 control to P188 control the 8088 will continue from where it left off.

To implement this change, proceed with the following steps:

1) Remove jumper E
2) Add a jumper from E1 to T1

We now have connected the output of flip-flop A1-9 to the *HOLD input to the 8088. Therefore, instead of setting the 8088 at the reset address when it is removed from the bus, it will do a processor HOLD. There is an adjustment to the software that goes along with this change. The software change is as follows:

ADDRESS	CODE	
XØ	E6, X	OUT PORT-X TRANSFER COMMAND
2	90	NOP --(Must be at least 4
3	90	NOP NOP's here.)
4	90	NOP
5	90	NOP
6	START OF CODE FOR CONTINUING WHEN TRANSFERRING BACK FROM Z80 CONTROL.	

The NOP's are necessary because timing differences with the Z80 and 8088 may cause one or more NOP's not to be executed after transfer from Z80 to 8088 control.

This change has run in ACOM's lab with a test that transfers control once every second for several hundred hours without one transfer failure. The test was done using dynamic RAM and a 4MHZ Z80. The test was done using the connections outlined in application note P188-1.

ACOM / Electronics

4151 Middlefield Rd. Palo Alto, Calif. 94303 (415) 494-7499

March 27, 1982

Dear Customer:

Enclosed please find application note P188-3. You should have received application note P188-1 and P188-2. If you have not received the two previous application notes, please let us know so we can send them out. This application note shows you how to jumper the P188 to run continuation transfers. This should make some applications easeier. We are working on more application notes. Currently in progress is one describing the use of the P188 in a North Star Computer.

Furthermore, any application information you wish to send us, we will assemble and pass on to our customers. We are currently developing a more advanced 8088 processor board. If you have any suggestions on what you would like to see on this card, please drop us a line. We are also developing other S100 bus cards, so keep us informed of any address change so we can keep you informed.

Sincerely,

Sam R. Hawes, Jr.

Sam R. Hawes, Jr.
ACOM Electronics

SRH/lh
Enclosure

We are in the process of designing an advanced P188 board. If you have any suggestion on what might be included on the board, please let me know. Also let me know if you have any problems in implementing the above change.

Sincerely,

Sam R. Hawes, Jr.
ACOM Electronics

SRH/lh

ACOM / Electronics

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ACOM ELECTRONICS-----APPLICATION NOTE P188-4

This application note describes how to jumper the P188 board so that when you transfer from Z80 control to P188 control the 8088 will continue from where it left off. This same function was accomplished in application note P188-3; however, it required NOP's to be added in the 8088 code. With the changes outlined in Fig. 2, full handshake is provided for the Z80 HOLD & HLDA lines and the 8088 HOLD & HLDA. Therefore, no NOP (CODE 90) need be used. Fig. 1 shows a schematic representation of the transfer circuit after installing the changes.

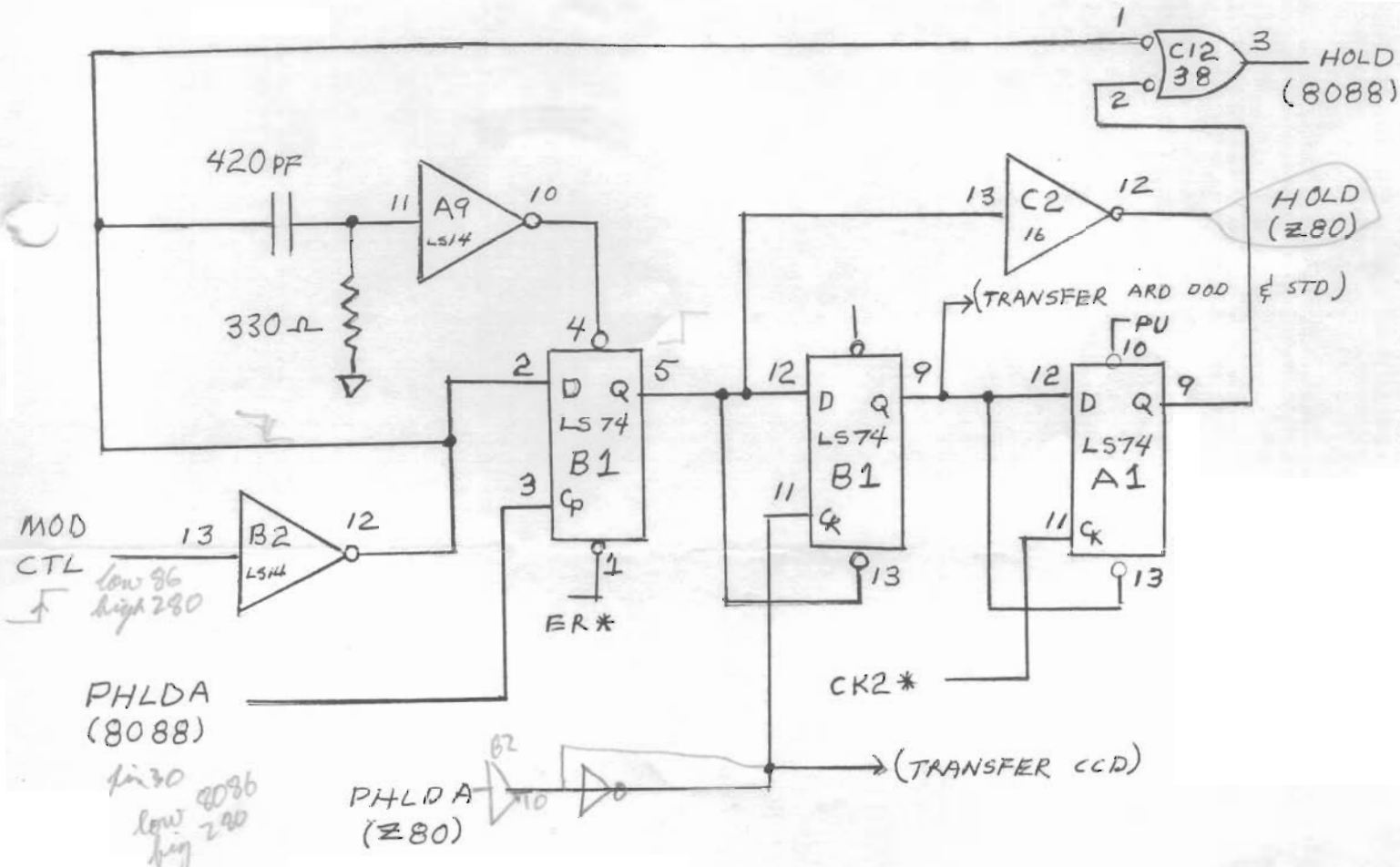


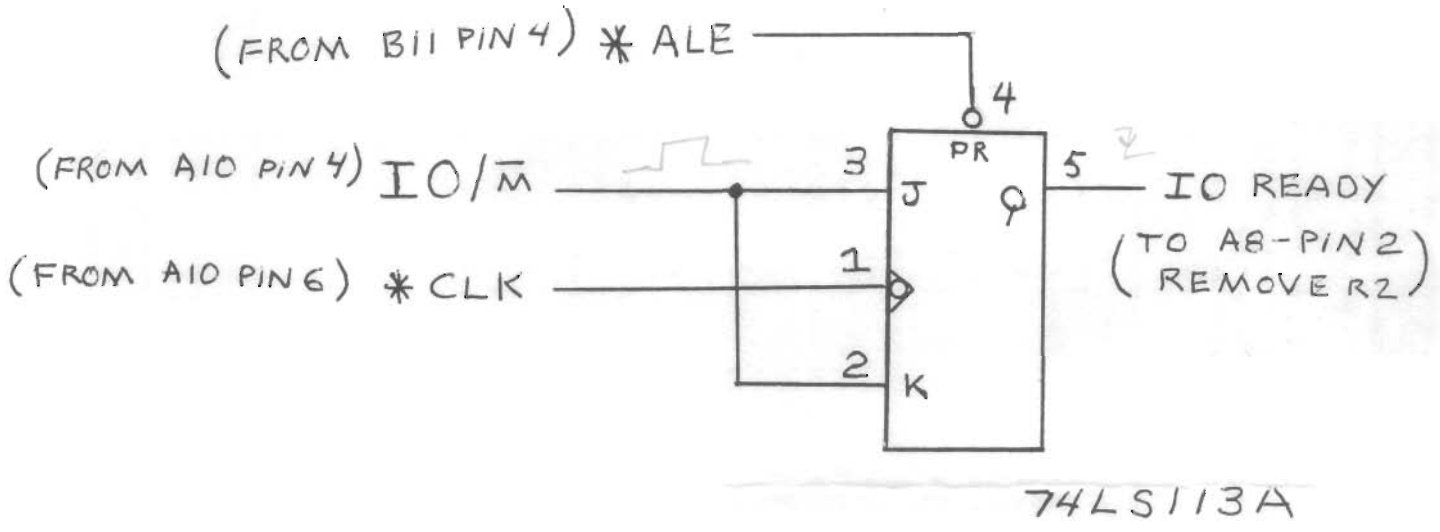
FIG. 1

ACOM ELECTRONICS------APPLICATION NOTE--P188-2

This application note describes how to add a wait state to IO operations. This is useful when running the P188 with a system that requires slow I/O or when the 8088 is running at 8 or 10 MHZ.

A 74LS 113A flip-flop is added to the P188 at one of the spare socket locations and connected as shown in Figure 1. This will cause one wait state for every IO cycle, but not memory cycles.

FIGURE 1



P188 CHANGES FOR 88 HOLD & HLDA HAND SHAKE

not mod P188-4 in rev 188-2

FIG. 2

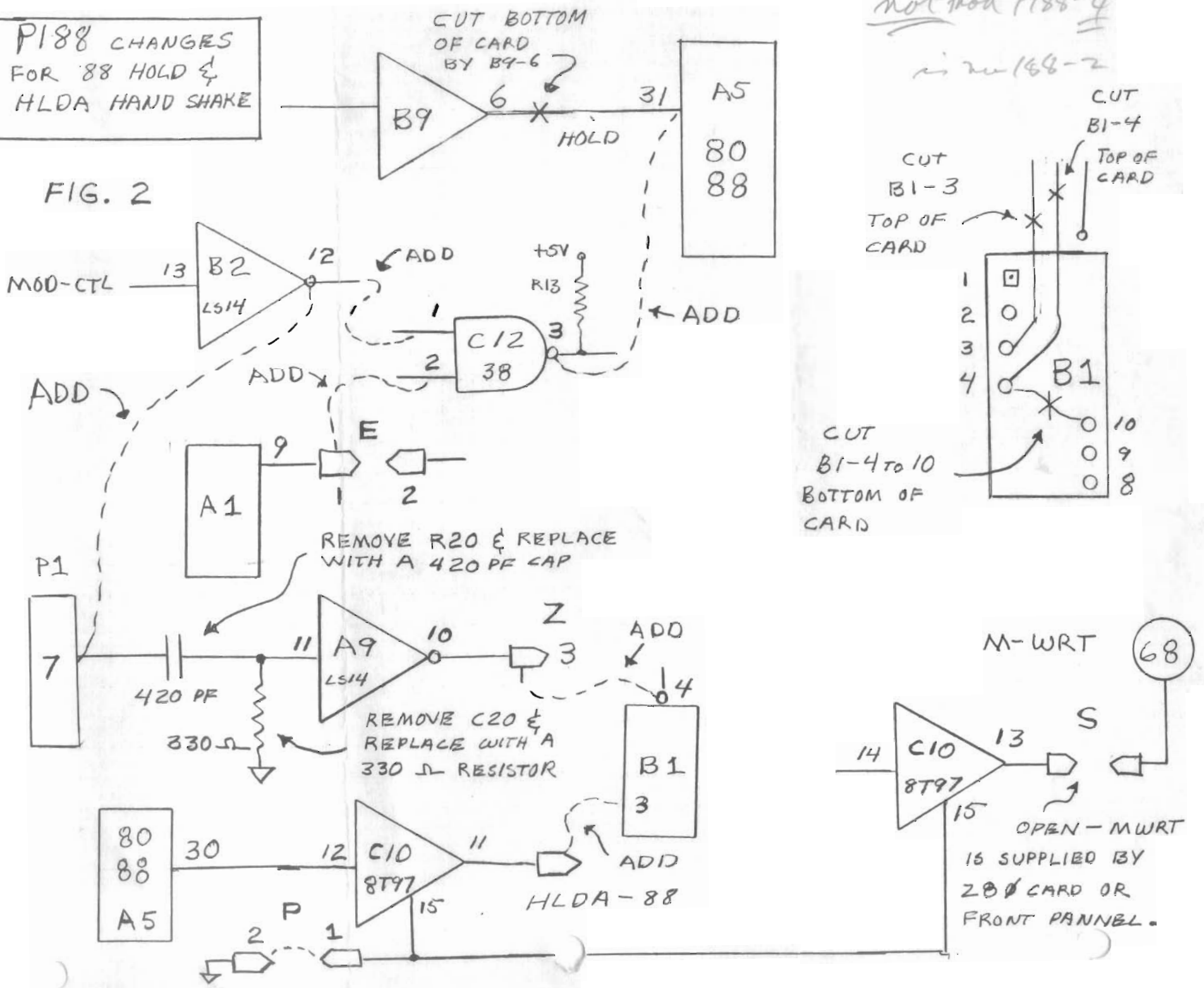
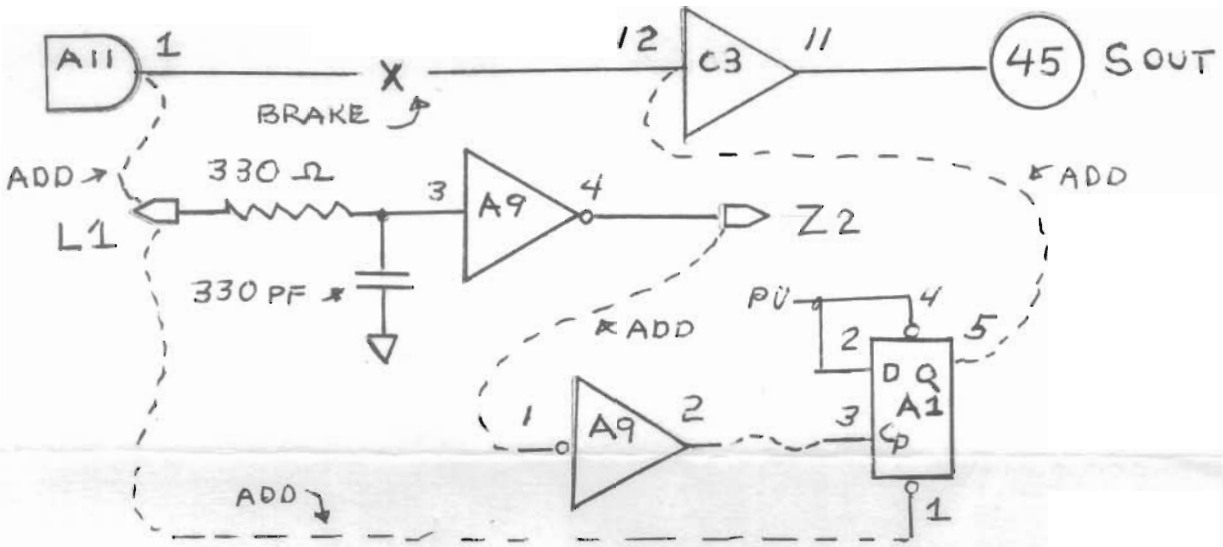
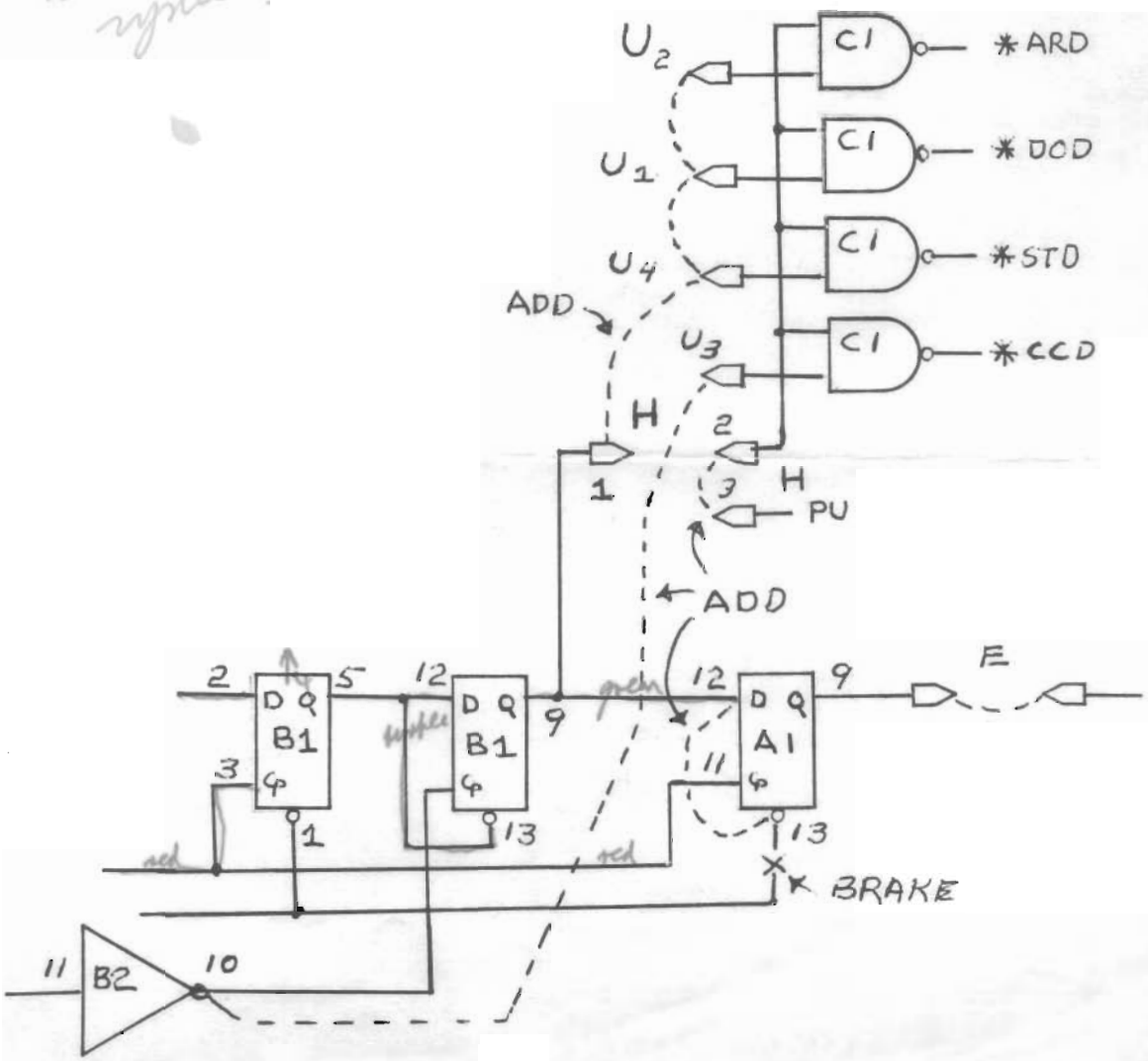


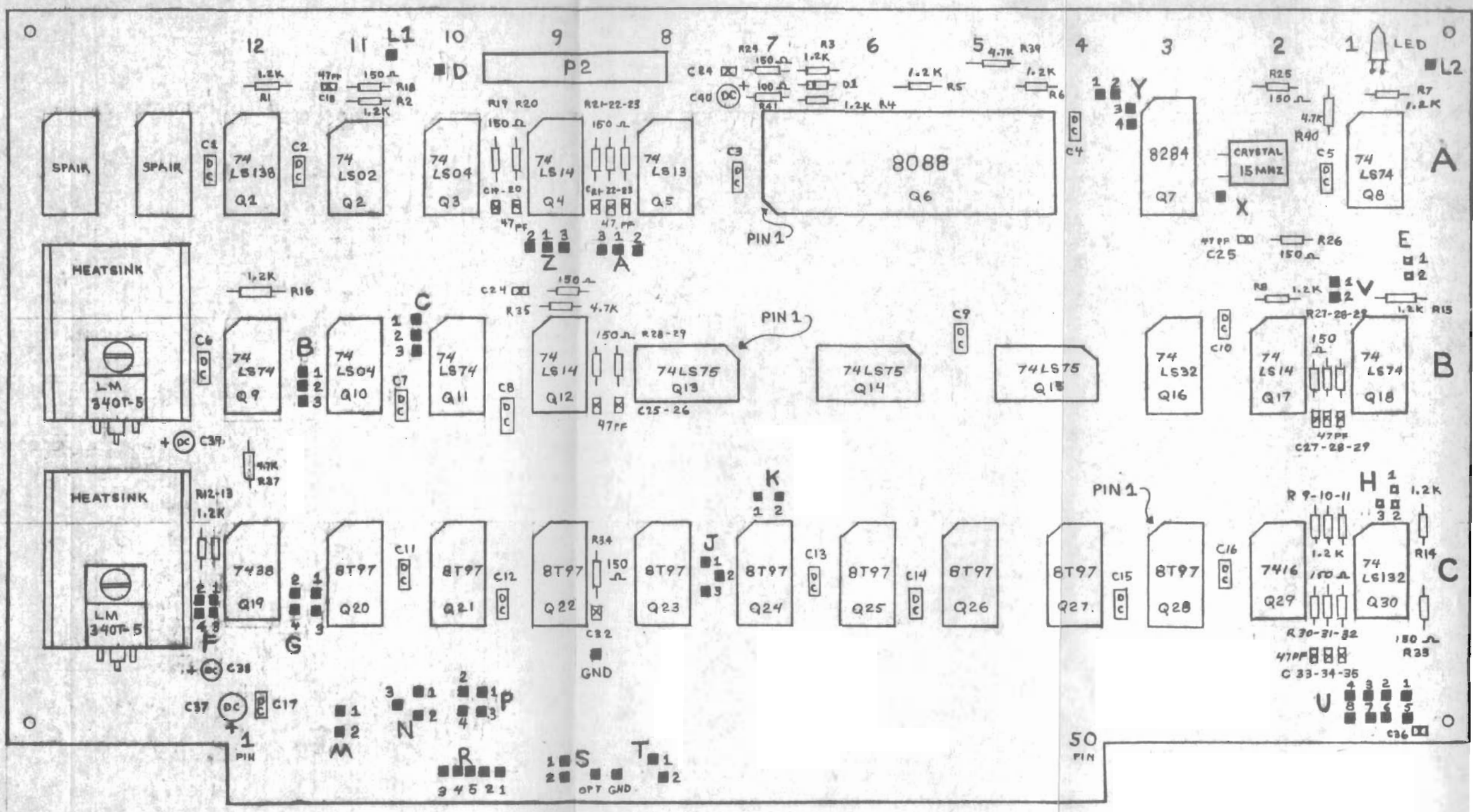
FIGURE 1

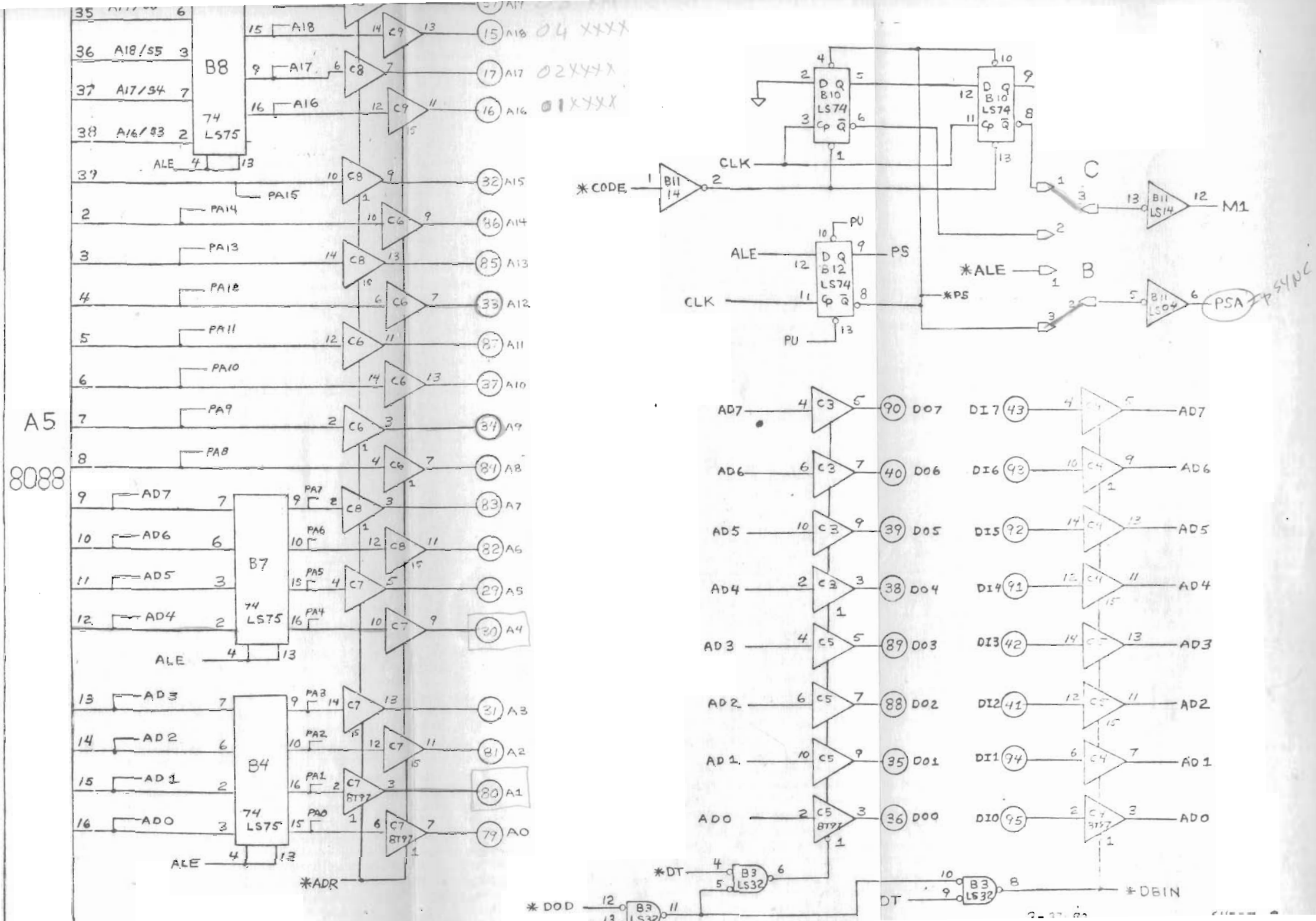


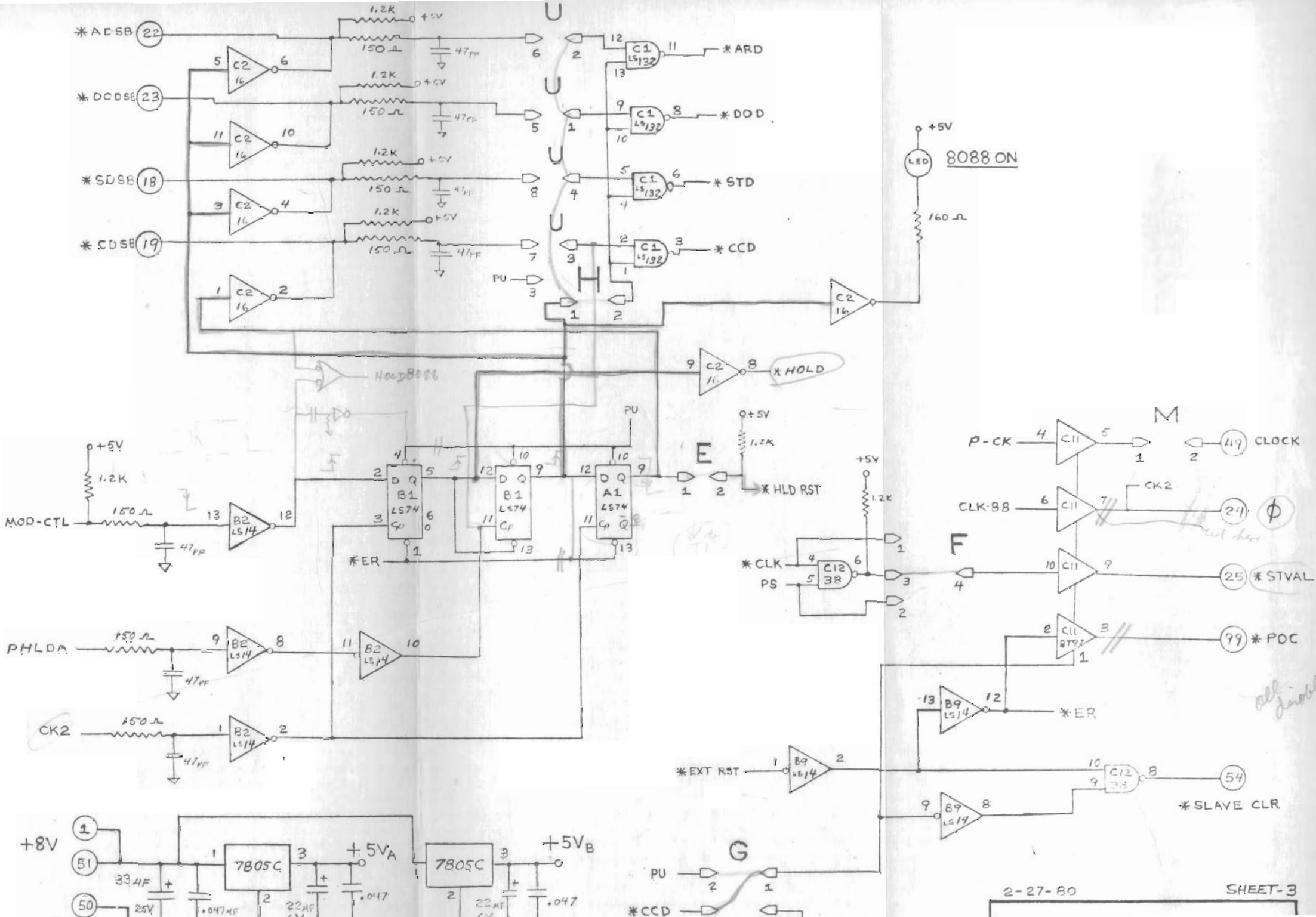
will not work with my system!

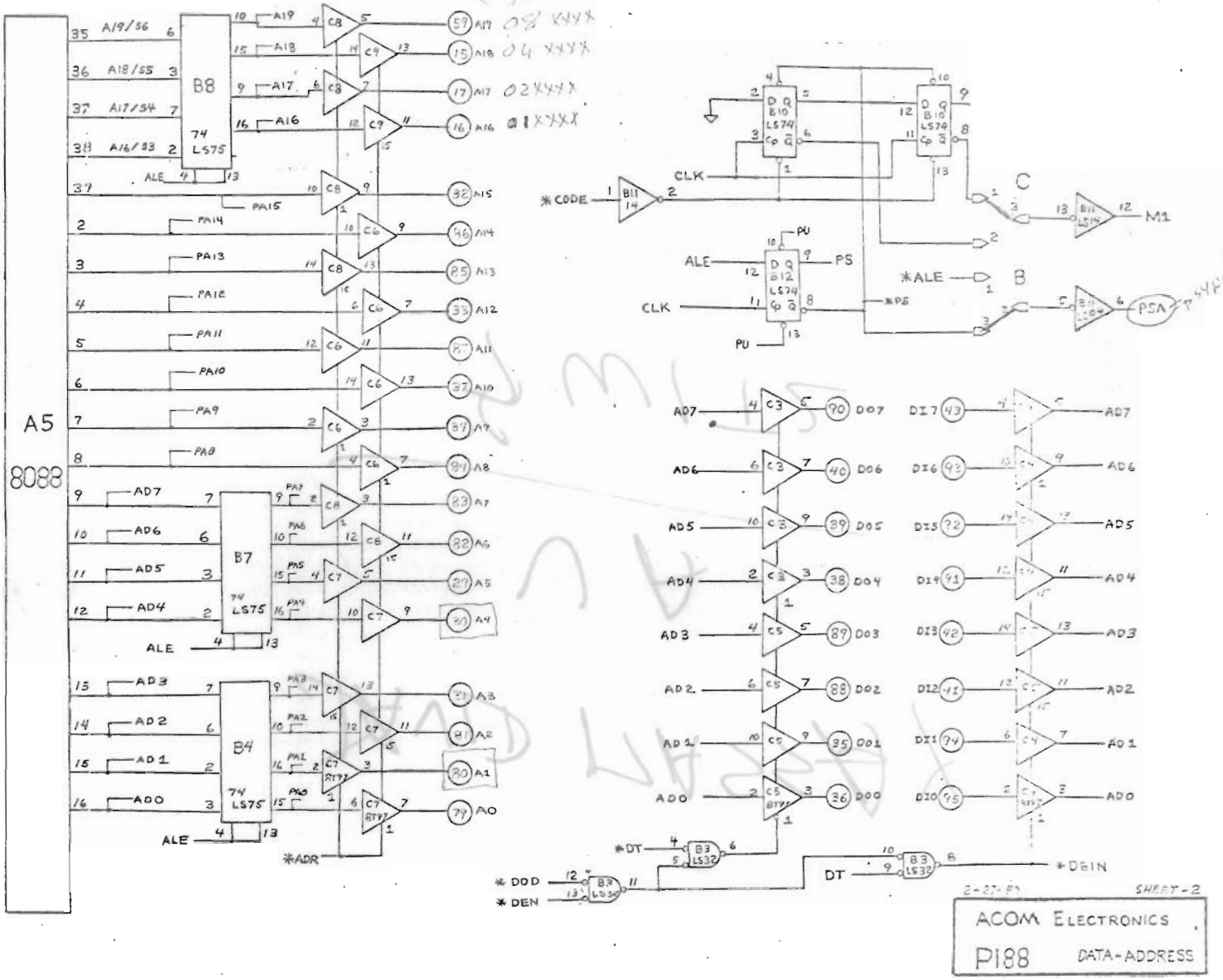
FIGURE 2

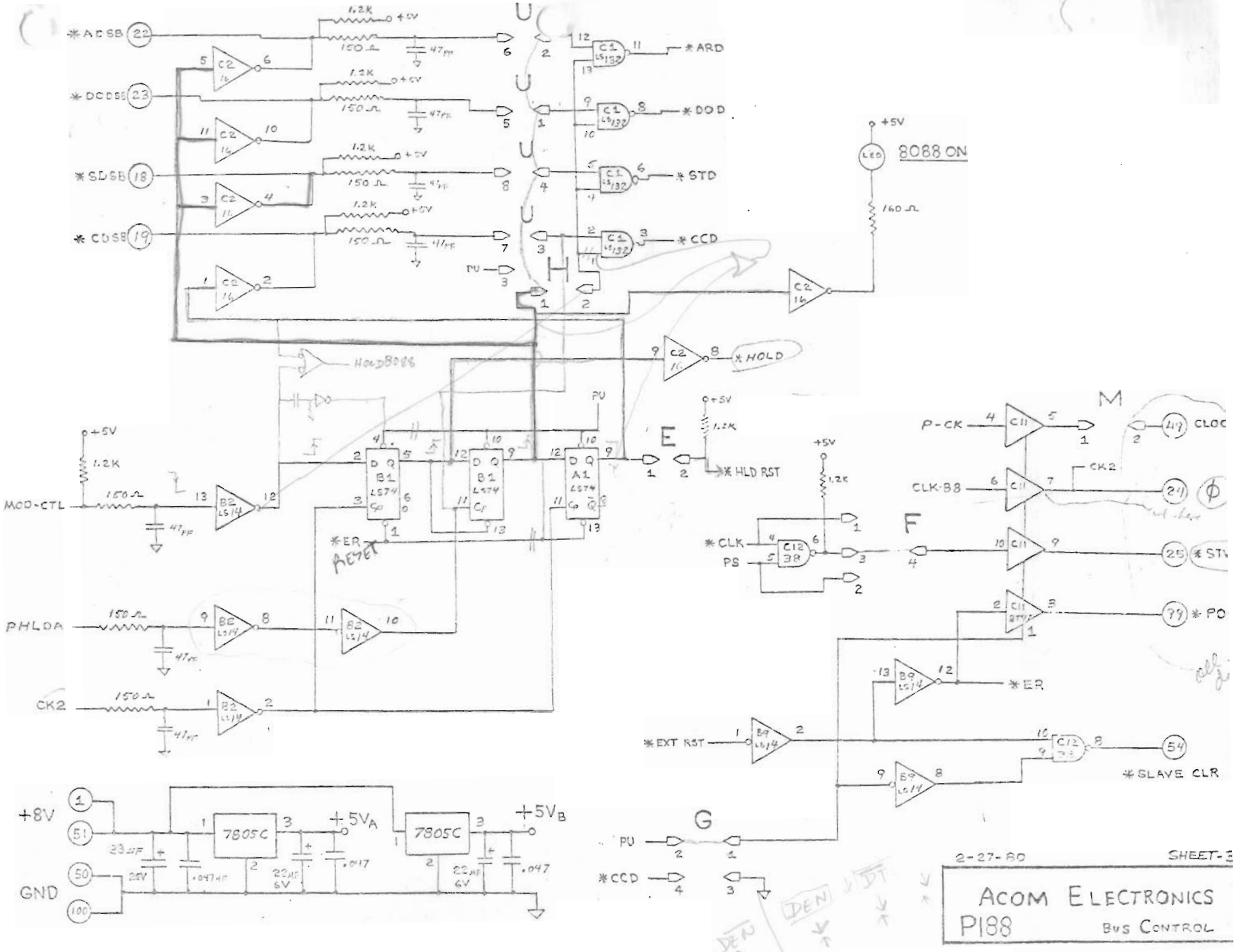



12 11 L1 10 9 8 7 6 5 4 3 2 1 LED L2
P2
SPAIR
SPAIR
74 LS138 Q1
74 LS02 Q2
74 LS04 Q3
74 LS14 Q4
74 LS13 Q5
8088 Q6
8284 Q7
CRYSTAL 15 MHZ
74 LS74 Q8
HEATSINK
LM 340T-5
74 LS74 Q9
74 LS04 Q10
74 LS74 Q11
74 LS14 Q12
74LS75 Q13
74LS75 Q14
74LS75 Q15
74 LS32 Q16
74 LS14 Q17
74 LS74 Q18
HEATSINK
LM 340T-5
7438 Q19
8T97 Q20
8T97 Q21
8T97 Q22
8T97 Q23
8T97 Q24
8T97 Q25
8T97 Q26
8T97 Q27
8T97 Q28
7416 Q29
74 LS132 Q30
PIN 1
PIN 1
GND
OPT GND
50 PIN
1 PIN
R1 1.2K
R2 1.2K
R3 1.2K
R4 1.2K
R5 1.2K
R6 1.2K
R7 1.2K
R8 1.2K
R9-10-11 1.2K
R12-13 1.2K
R14 1.2K
R15 1.2K
R16 1.2K
R18 150Ω
R19 R20 150Ω
R21-22-23 150Ω
R24 150Ω
R25 150Ω
R26 150Ω
R27-28-29 150Ω
R30-31-32 150Ω
R33 150Ω
R34 150Ω
R35 4.7K
R36 4.7K
R37 4.7K
R39 4.7K
R40 4.7K
R41 100Ω
C18 47pf
C19-20 47pf
C21-22-23 47pf
C24 150pf
C25 47pf
C25-26 47pf
C27-28-29 47pf
C33-34-35 47pf
C36 .047μf
C37 22μf 6V
C38 22μf 6V
C40 22μf 6V
C17 33μf 25V
= .047μf
= 47pf
22μf 6V
33μf 25V
= TYP. JUMPER GROUP


A5
8088
B8
74 LS575
B7
74 LS75
B4
74 LS75
ALE
PA15
PA14
PA13
PA12
PA11
PA10
PA9
PA8
PA7
PA6
PA5
PA4
PA3
PA2
PA1
PA0
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
A18
A17
A16
A18/S5
A17/S4
A16/S3
*ADR
*CODE
CLK
PU
PS
*ALE
*PS
M1
PSA = PSYNC
*DT
*DOD
DT
*DBIN
DO7
DO6
DO5
DO4
DO3
DO2
DO1
DO0
DI7
DI6
DI5
DI4
DI3
DI2
DI1
DI0


*ADSB 22
*DDSB 23
*SDSB 18
*CDSB 19
1.2K
+5V
150Ω
47pF
C2 16
C1 LS132
*ARD
*DOD
*STD
*CCD
PU
HOLD8088
*HOLD
LED
8088 ON
160Ω
MOD-CTL
B2 LS14
D Q B1 LS74 Cp
A1 LS74 Cp Q̄
*ER
*HLD RST
PHLDA
CK2
*CLK
PS
C12 38
P-CK
C11
CLOCK
CLK-88
CK2
Φ
*STVAL
*POC
B9 LS14
*EXT RST
*SLAVE CLR
+8V
7805C
+5VA
+5VB
33μF
25V
.047μF
22μF
.047
G
*CCD
H
E
F
M
2-27-80
SHEET-3


A5
8088
B8
74 LS575
B7
74 LS575
B4
74 LS575
ALE
*ADR
CLK
*CODE
PU
ALE
PS
*ALE
*PS
PSA
M1
*DT
*DOD
*DEN
DT
*DBIN
2-27-85
SHEET-2
ACOM ELECTRONICS
P188 DATA-ADDRESS


*ACSB
*DCDSB
*SDSB
*CDSB
*ARD
*DOD
*STD
*CCD
PU
HoldB086
*HOLD
8088 ON
+5V
MOD-CTL
PHLDA
CK2
*ER
RESET
*HLD RST
*CLK
PS
P-CK
CLK-88
*EXT RST
*SLAVE CLR
+8V
GND
+5VA
+5VB
7805C
2-27-80
SHEET-3
ACOM ELECTRONICS
P188
BUS CONTROL