Trident

TVGA9000i
LOW COST VGA CONTROLLER

Features

- Fully integrated, low cost solution for IBM PC/AT and PS/2 and compatibles
- Supports 800x600, 1024x768 (interlaced or non-interlaced), and 768x1024 in 16 colors
- Supports 640x400, 640x480, 800x600 in 256 colors
- Integrated display DAC
- Integrated clock synthesizer with programmable frequencies up to 80MHz
- Built-in data bus transceiver and Feature Connector support
- Only two 256Kx4 DRAM required for complete VGA board solution
- Supports up to 512K of DRAM
- Fully hardware compatible with IBM VGA modes
- Fully hardware compatible with EGA, CGA, MDA, and Hercules™ at the register level
- Supports 132-column text in 25, 30, 43, or 60 rows
- Only one 32KB EPROM required to achieve 16-bit BIOS operation
- 1µm low power CMOS technology
- 160 pin, PFP package

General Description

The TVGA9000i is the ultimate low cost, high performance VGA solution. A complete VGA solution has been integrated into a single chip. This extremely small footprint design is ideal for motherboard designs and low cost adapters. The key to this small footprint is the integrated clock synthesizer and display DAC. The integrated clock synthesizer supplies 16 selectable VCLK frequencies up to 80MHz. The integrated display DAC supports 640x400, 600x480, and 800x600 in 256 colors; and 800x600 and 1024x768 in 16 colors. The DAC palette may be set for 256/256K colors. To further reduce the footprint, the data bus transceivers have been built into the chip. The result is a chip which requires only DRAM for a complete video subsystem design.

The TVGA9000i is versatile and full-featured. The chip provides register-level compatibility, enhanced graphics and text modes, support for 256Kx4 DRAM, plasma display control, and support for analog VGA, EGA, CGA, and MDA monitors. Register-level design insures compatibility with standard IBM VGA modes, and backward compatibility with EGA, CGA, MDA, and Hercules™ modes. The enhanced graphics modes provide high-resolution displays in 16 and 256 colors.

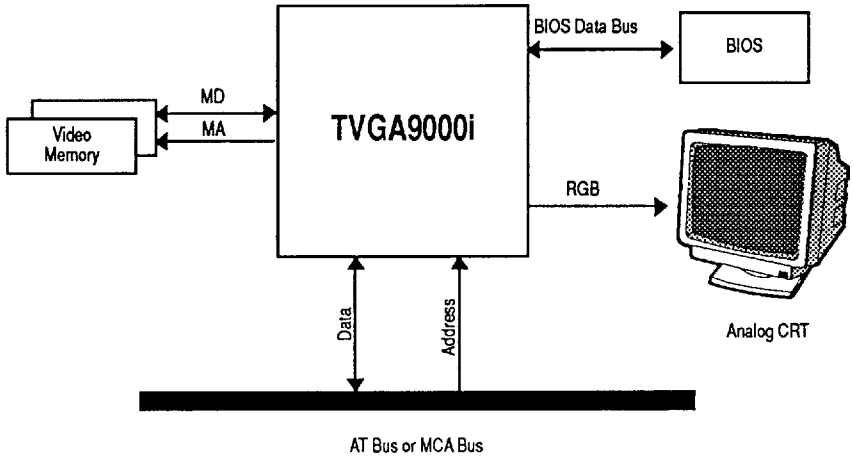

Figure 1. TVGA9000i Functional Block Diagram

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Compatibility

The TVGA9000i is fully compatible with all standard IBM VGA modes, EGA, MDA, and Hercules™ modes, and allows:

- Use of application software that uses any of the above modes
- Emulation of EGA, MDA, and Hercules™ modes on a VGA monitor

Extended Graphics and Text Modes

Extended graphics modes support includes:

- 640x400, 640x480 and 800x600 in 256 colors from a palette of 256K colors
- 800x600 and 1024x768 (interlaced and non-interlaced) in 16 colors from a palette of 256K colors
- Extended text modes offer 132-column text with 25, 30, 43, and 60 rows

Table 1 outlines the amount and the speed of Fast Page DRAM Mode 256Kx4 DRAM required to implement the 16 and 256 color modes.

Table 1. 16, 256-Color DRAM Requirements

	Colors			DRAM Count		Speed ns	
Resolution	4	16	256	2	4	100	80
Standard VGA		•		•			•
640x480 (Non-interlaced)			•		•		•
800x600 (Non-interlaced)		•		•			•
800x600 (Interlaced)			•		•	•	
800x600 (Non-interlaced)			•		•	•	
1024x768 (Non-interlaced)	•			•			•
1024x768 (Interlaced)		•			•	•	
1024x768 (Non-interlaced)		•			•		•

Hardware Features

The TVGA9000i offers the following special hardware features:

- Integrated anti-sparkle display DAC
- Programmable internal video clock up to 80MHz
- Source address register to speed memory read/write
- Optimized IOCHRDY Line to speed CPU access
- All TTL included in chip
- 16-bit BIOS operation requires only one 32KB EPROM

Software Drivers Supported

Extended graphics and text modes are supported by software application drivers developed by Trident. The following applications are supported:

- AutoCAD
- Autoshade
- CADKEY
- Framework
- GEM
- Lotus
- MS Windows
- MS Word
- P-CAD
- Symphony
- Ventura
- VersaCAD
- WordPerfect
- Wordstar
- OS/2
- SCO X-Windows (contact SCO)
- Quattro Pro
- Edsun CEG™ (Windows, AutoCAD, Lotus)
- 8514/AI Emulation
- VESA BIOS Extension

Contact Trident for the latest high-resolution driver releases.

TVGA9000i Applications

The TVGA9000i works with your hardware to allow you to develop a cost efficient, high performance system. The TVGA9000i can be used to implement specific applications such as small footprint solutions for motherboards or low cost VGA adapters.

A minimum configuration requires a TVGA9000i, two 256Kx4 DRAM chips, 32KB EPROM, 15-pin connector, 40 MHz crystal, jumpers, and miscellaneous ferrite beads, capacitors, resistors.

TVGA9000i Components

The TVGA9000i consists of eight major components: Sequencer, CRT Controller, Graphics Controller, Attribute Controller, Host Bus Interface, Display Memory Bus Interface, Clock Synthesize, and Display DAC. These components are used to generate video output and timing for video memory and the monitor.

Sequencer

The sequencer provides basic memory timing for DRAM interfacing, and a character clock for the CRTC and for controlling regenerative memory fetch. The sequencer uses a 32 byte video cache to let the CPU access display memory during active display intervals. Video data from the cache can be output to the video screen while the CPU accesses video memory. This greatly increases performance over standard CPU access implementations.

CRT Controller

The CRT (Cathode Ray Tube) Controller provides complete control for horizontal and vertical synchronous timing, address interface between video memory and display screen, cursor and underline timing, and refresh addressing for dynamic RAMs.

Graphics Controller

During the active display interval, the Graphics Controller directs data from video memory to the Attribute Controller. In graphics modes, memory data is formatted into serialized form and sent to the Attribute Controller. In text mode, the parallel attribute byte goes directly to the Attribute Controller without going through the Graphics Controller. During video memory read/write operations, the Graphics Controller acts as an interface to the CPU. The Graphics Controller can perform logic operations on memory data before it reaches the display memory or system data bus.

Attribute Controller

The Attribute Controller takes in data from video memory and formats it for output on the display monitor. In addition, the Attribute Controller takes care of blinking, underlining, cursor insertion, and PEL panning. In text mode, 16 bits of code are divided into 8 bits of character code and 8 bits of attribute code. The character code is used as a look-up into a font table. The attribute code is used to determine character color, blinking, bold, etc. In graphics mode, the Graphics Controller serializes memory bits. Each output color is translated through the internal color palettes and then sent to the DAC. Here it is used as an address to the 18/24-bit color look-up table. The value read from the color look-up table is converted into three analog signals (R, G, B) for driving an analog display.

Host Bus Interface

The TVGA9000i supports the PC/AT and the Micro Channel bus by setting or resetting select configuration bits during the system reset time. When the TVGA9000i is part of the Micro Channel board solution, several host bus interface pins are defined or designated differently from a PC/AT solution.

The BIOS PROM data width can be configured as 16-bit or 8-bit at system reset time by pulling MD7 high or low, respectively. If the 16-bit mode is turned on, the TVGA9000i will return $\overline{MCS16}$ when the PROM is addressed. If the on-board BIOS is not used, the PROM chip(s) can be disabled by pulling MD6 low at system reset time. The TVGA9000i supports up to 32KB BIOS, which is located at the address hex C0000-C7FFF. For additional system reset configuration definitions, see "Definitions of MD7-MD0 and RMD7-RMD0 at System Reset" section on the next page.

The TVGA9000i can address up to 512KB of video memory depending on the mode (text or graphics). The 16-bit-wide data bus can be activated automatically by BIOS. The TVGA9000i will drive $\overline{MCS16}$ when the 16-bit mode is set and the video memory is accessed. In order to comply with the Micro Channel specifications, the TVGA9000i supports channel ID (I/O address 100 and 101), as well as the card-enable control bit (bit 0 of I/O port 102). When the video memory or the on-board I/O registers are accessed, the TVGA9000i responds with $\overline{CD\ SFDBK}$.

Display Memory Bus Interface

The TVGA9000i provides a bus interface for the video display DRAM. The interface provides address multiplexing, data multiplexing, refresh, and $\overline{RAS}$, $\overline{CAS}$, and write-enable signals. Eighteen address pins (MAA8-MAA0 for Bank A and MAB8-MAB0 for Bank B) and 32 data pins (MD23-MD16, MD7-MD0) are available for display memory.

Clock Synthesizer

The built-in clock synthesizer provides up to 16 selectable internal video clock frequencies (up to 80MHz). The 16 selectable frequencies can be programmed through Trident's special VGA registers. Please refer to Table 2 for dot clock frequency outputs.

Table 2. TVGA9000i Video Clock Generator Frequencies

Selectable Frequencies				
25.175[1]	28.322[1]	36.000	44.900[1]	50.350
57.270	62.400	65.000	72.000	75.000
77.000	80.000	40.000		

[1] This value used twice

Display DAC

The display DAC has three 6-bit DACs, and a 256x18 Color Look-up Table (LUT). The DAC can generate RS-343A compatible red, green, and blue signals into a doubly terminated 75Ω load without external buffering. RS-170 compatible video signals may also be generated into a single terminated 75Ω without external buffering. The DAC output current may be set by using an external or internal voltage reference together with full scale adjustment.

The Color Look-up Table (LUT) may be programmed with 256, 6-bit RGB values. The LUT table may be directly accessed.

MD & RMD Defintions at System Reset

Table 3 and 4 list the definition for MD7-MD0 and RMD7-RMD0 at system reset.

Table 3. MD7-MD0 Definitions

MD	Logic Value[1]	Definition
MD7	0	8-bit BIOS
	1	16-bit BIOS
MD6	0	ROM disable
	1	ROM enable
MD5	0	I/O port at 2xx
	1	I/O port at 3xx
MD4	0	MCA bus
	1	PC bus
MD3-0	*	External switch settings

[1]Set a Logical 0 value by pulling-down to GND through a 4.7K-10K resistor. No pull-up resistor required for a Logical 1 value.

[2]Data is read into a 4-bit resistor. The data values can be used by the BIOS or application software.

Table 4. RMD7-RMD3, RMD1, and RMD0 Definitions

MD	Logic Value[1]	Definition
RMD7	0	8-bit video memory access
	1	16-bit video memory access
RMD6	0	Internal clock chip enable
	1	External clock chip disable
RMD5	0	256Kx4 memory (4 chips)
	1	256Kx4 memory (2 chips)
RMD4	0	Selects 46E8 for port control
	1	Selects 3C3 for port control
RMD3	0	24K BIOS
	1	32K BIOS
RMD1	0	Enables ISA/MCA bus interface
	1	Reserved
RMD0	0	Uses SA lines to decode $\overline{\text{MCS16}}$
	1	Uses LSA19-17 to decode $\overline{\text{MCS16}}$

[1]Set a Logical 0 value by pulling-down to GND through a 4.7K-10K resistor. No pull-up resistor required for a Logical 1 value.

Chip Specifications

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Type	Maximum	Units
Power Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Input Voltage	V_{IN}	GND		V_{DD}	V
Pin Voltage with respect to GND	V_{PIN}	-0.5		V_{DD}+0.5	V
Operating Temperature		T_{OP}	0	70	°C
Storage Temperature	T_{STO}	-40		100	°C

Stresses above those listed under MAXIMUM (Absolute Maximum Ratings) may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods make effect device reliability.

Table 6. DC Specifications

Parameter	Symbol	Minimum	Maximum	Units	Conditions
Input Low Voltage	V_{IL}	GND	0.8	V	V_{DD}=5V
Input HighVoltage	V_{IH}	2.0	V_{DD}	V	V_{DD}=5V
Input Low Current	I_{IL}	-	-0.5	µA	V_{IN}=0.0V
Input High Current	I_{IH}	-	20	µA	V_{IN}=V
Output Low Voltage	V_{OL}	-	0.4	V	See Note 1
High Voltage	V_{OH}	2.4	-	V	See Note 1
Impedance Leakage	I_{OZ}	-	10.0	µA	$V_{SS}<V_{OUT}<V_{DD}$
Supply Current	I_{OC}	-	195.0	mA	V_{DD}=5.25V(V_{DD}MAX)
DAC Output Level	-	-	700	mV	-

Note 1: I_{OL}/I_{OH}=4.5/-4.5mA for RMD7-RMD0, CLK1/SC3, CLK2/SC1, CLK3/SC2

I_{OL}/I_{OH}=9/-9mA for SD15-SD0, IRQ, $\overline{\text{ROMCS}}$, VSYNC, HSYNC, MAA8-MAA0, MAB8-MAB0, MD23-MD16, MD7-MD0, $\overline{\text{WE2}}$, $\overline{\text{WE0}}$, $\overline{\text{CASA}}$, $\overline{\text{RAS}}$, ROMBA0, OUTP0, $\overline{\text{MSC16}}$, CLK0, DMCLK

I_{OH}=14mA for R,G,B

I_{OL}/I_{OH}=18/-18mA for IOCHRDY

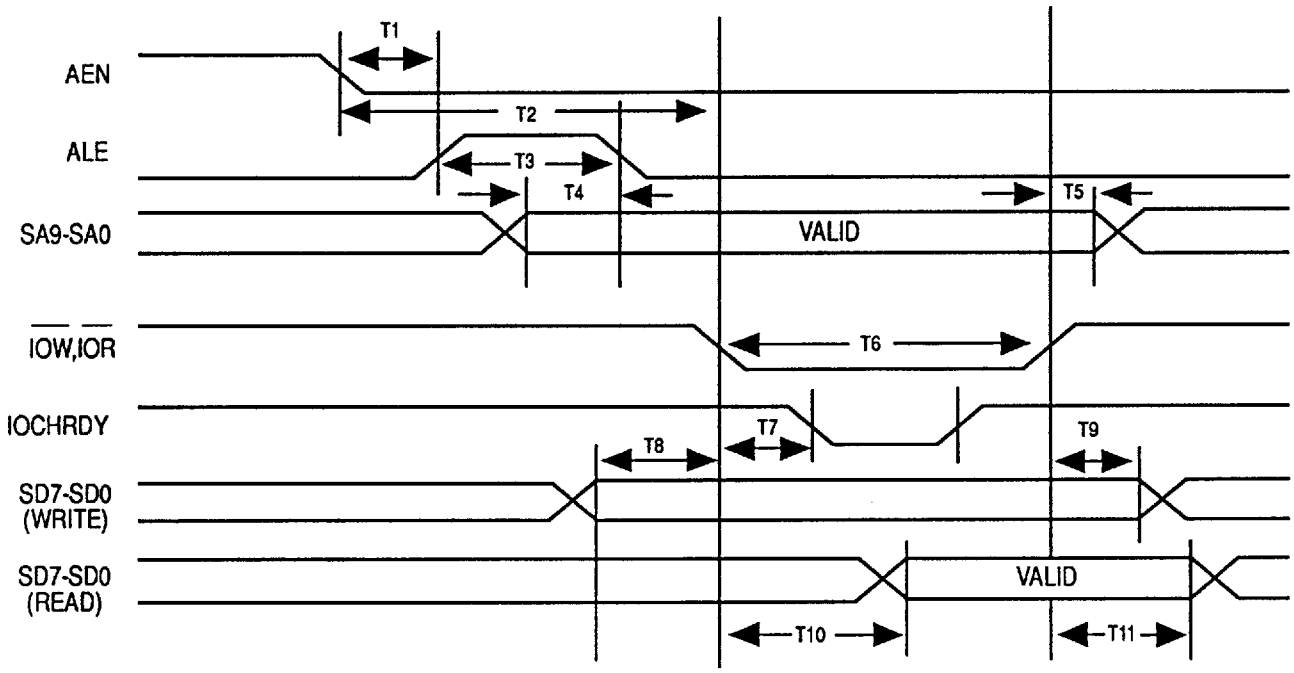

Figure 2. PC/AT ISA Bus I/O Read/Write Timing

Table 7. AC Specifications for ISA Bus I/O Read/Write in Nanoseconds

SYM	Description	Min	Typ	Max
T1	AEN Valid to Rising Edge of ALE	100		
T2	AEN Valid to I/O Command Active	5		
T3	ALE Active to Inactive	15.5		
T4	SA9-SA0 & $\overline{SBHE}$ Valid to Falling Edge of ALE	29.5		
T5	SA9-SA0 & $\overline{SBHE}$ Valid Hold From Command Inactive	18		
T6	I/O Command Active		60	
T7	IOCHRDY Inactive From Active Command	10		15
T8	Valid Write Data Setup to I/O Command Active	4.5		80
T9	Write Data Valid Hold From I/O Command Inactive		30	
T10	Read Data Valid From Read Command Active			60
T11	Read Command Inactive to SD7-SD0 Invalid			20

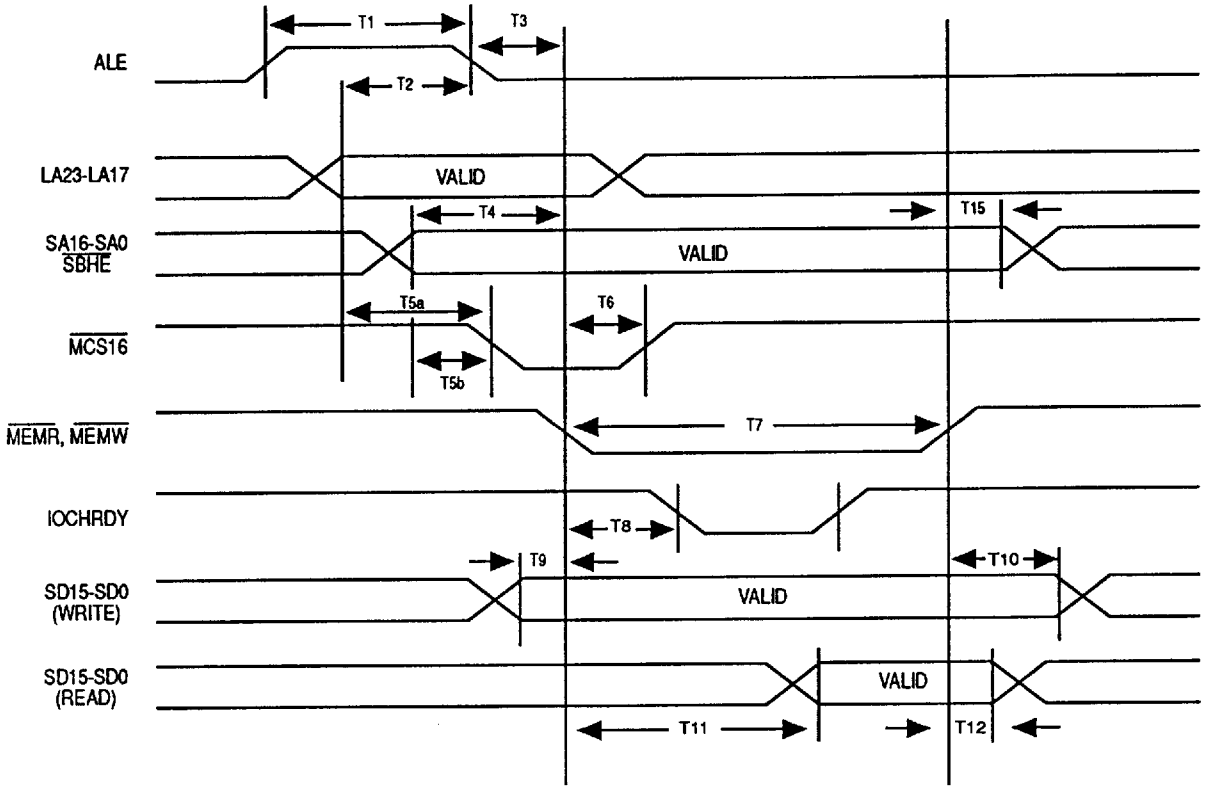

Figure 3. PC/AT ISA Bus Memory Read/Write Timing

Table 8. AC Specifications for ISA Bus Memory Read/Write In Nanoseconds

SYM	Description	Min	Typ	Max
T1	ALE Active to Inactive	15		
T2	LA23-LA17 Valid Setup to Falling Edge of ALE	20		
T3	ALE Inactive to Command Active	20		
T4	SA16-SA0 & $\overline{\text{SBHE}}$ Valid to Memory Command Active	5		
T5a	$\overline{\text{MCS16}}$ Active From Unlatched Address			20
T5b	$\overline{\text{MCS16}}$ Active From Latched Address			14
T6	$\overline{\text{MCS16}}$ Valid Hold From Invalid LA23-LA17			25
T7	Memory Command Active to Inactive	80		
T8	IOCHRDY Inactive From Memory Command Active	10		20
T9	Valid Write Data Setup to Memory Command Active	0		
T10	Write Data Valid Hold From Memory Command Inactive	10		
T11	Valid Read Data From Memory Command Active	0		
T12	Read Command Inactive to SD15-SD0 Invalid			20
T15	Latched Address Hold Time After Command	0		

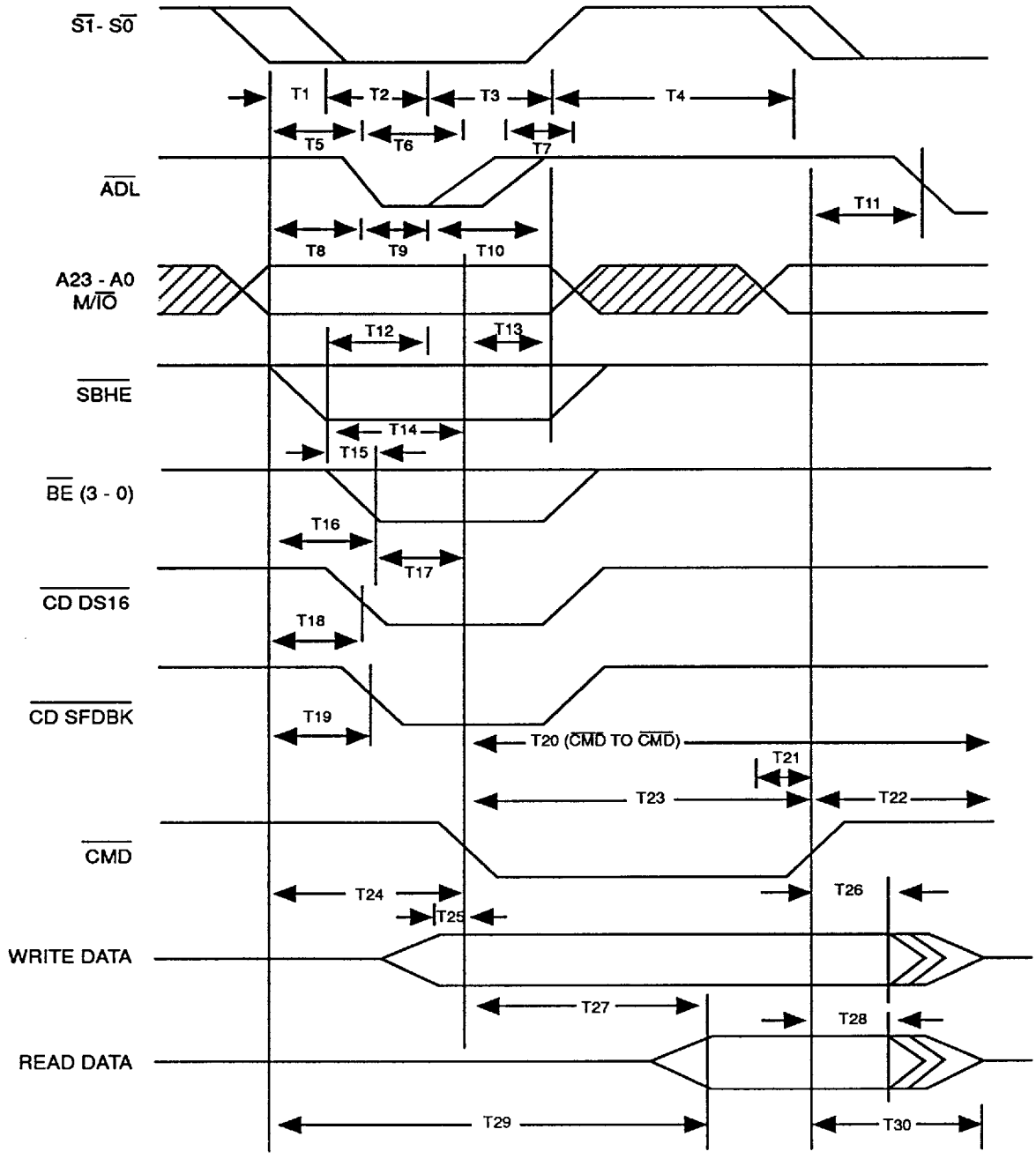

Figure 4. Micro Channel Bus Timing

Table 9. AC Specifications for MCA Bus in Nanoseconds

SYM	Description	Min	Typ	Max	
T1	Status Active From ADDRESS, M/$\overline{IO}$, $\overline{REFRESH}$	10			
T2	$\overline{CMD}$ Active From Status Active	55			
T3	Status Hold From $\overline{CMD}$ Active	30			
T4	Next Status Active From Status Inactive			30	
T5	$\overline{ADL}$ Active From ADDRESS, M/IO, REFRESH	45			
T6	ADL Active to $\overline{CMD}$ Active	40			
T7	ADDRESS, M/$\overline{IO}$, $\overline{REFRESH}$, $\overline{SBHE}$ hold from $\overline{ADL}$ Inactive		25		
T8	$\overline{ADL}$ Active from Status Active	12			
T9	$\overline{ADL}$ Active to Inactive		40		
T10	Status Hold From $\overline{ADL}$ Inactive	25			
T11	$\overline{CMD}$ Inactive to next $\overline{ADL}$ Active	40			
T12	$\overline{SBHE}$ Setup to $\overline{ADL}$ Inactive	40			
T13	ADDRESS, M/$\overline{IO}$, $\overline{REFRESH}$, $\overline{SBHE}$ hold from $\overline{CMD}$ Active		30		
T14	$\overline{SBHE}$ Setup to $\overline{CMD}$ Active	40			
T15	$\overline{BE3}$-$\overline{BE0}$ Active From $\overline{SBHE}$, A0, A1 Active			30	
T17	$\overline{BE3}$-$\overline{BE0}$ Active to $\overline{CMD}$ Active	10			
T18	$\overline{CD\ DS\ 16}$ Active (n) From $\overline{ADDRESS}$, M/$\overline{IO}$, $\overline{REFRESH}$ Valid				55
T19	$\overline{CD\ SFDBK}$ Active From $\overline{ADDRESS}$, M/$\overline{IO}$, $\overline{REFRESH}$ Valid				60
T20	$\overline{CMD}$ Active to Next $\overline{CMD}$ Active	190			
T21	Next Status Active to $\overline{CMD}$ Inactive		20		
T22	$\overline{CMD}$ Inactive to Next $\overline{CMD}$ Active	80			
T23	$\overline{CMD}$ Active to Inactive		90		
T24	$\overline{CMD}$ Active From Address Valid	85			
T25	Write Data Setup to $\overline{CMD}$ Active	0			
T26	Write Data Hold From $\overline{CMD}$ Inactive	30			
T27	Read Data Valid From $\overline{CMD}$ Active		60		
T28	Read Data Hold From $\overline{CMD}$ Inactive	0			
T29	Status to Read Data Valid			125	
T30	Read Data Bus Tri-state From $\overline{CMD}$ Inactive			40	

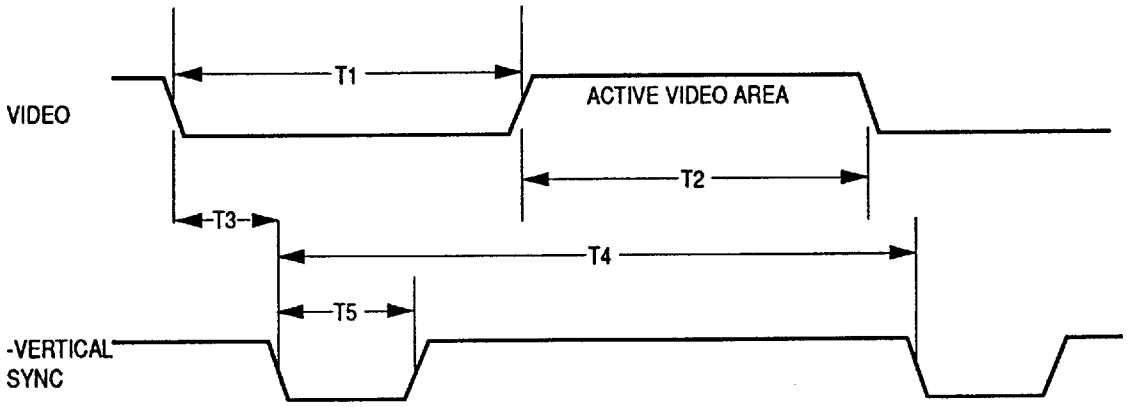

Figure 5. Vertical Timing

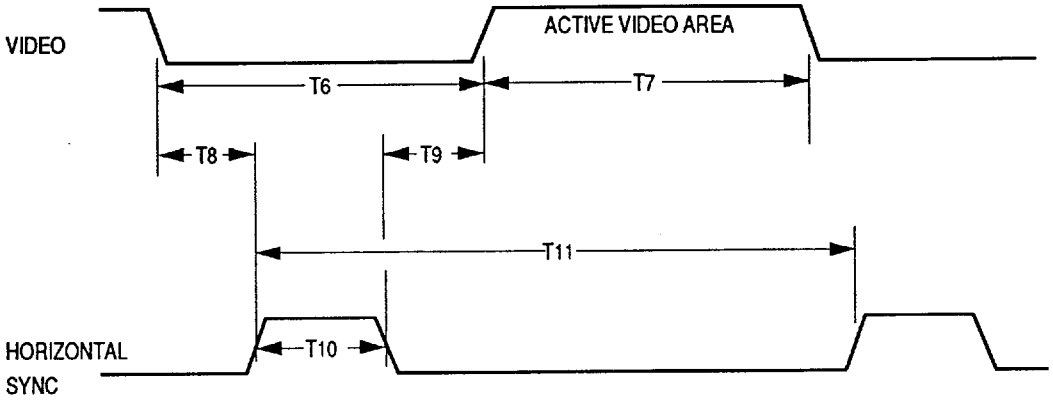

Figure 6. Horizontal Timing

Table 10a. Horizontal Timing (µsec)

MODE	CLK	TYPE	DISPLAY	MAX COLORS	T6	T7	T8	T9	T10	T11	POLARITY
0,1	25.2	A/N	40x25	16	6.356	25.422	0.636	1.907	3.813	31.778	-
2,3	25.2	A/N	80x25	16	6.356	25.422	0.636	1.907	3.813	31.778	-
0*,1*	25.2	A/N	40x25	16	6.356	25.422	0.636	1.907	3.813	31.778	+
2*,3*	25.2	A/N	80x25	16	6.356	25.422	0.636	1.907	3.813	31.778	+
0+,1+	28.3	A/N	40x25	16	6.356	25.422	0.636	1.907	3.813	31.778	-
2+,3+	28.3	A/N	80x25	16	6.356	25.422	0.636	1.907	3.813	31.778	-
4,5	25.2	APA	320x200	4	6.356	25.422	0.636	1.907	3.813	31.778	-
6	25.2	APA	640x200	2	6.356	25.422	0.636	1.907	3.813	31.778	-
7	28.3	A/N	80x25	Mono	6.356	25.422	0.636	1.907	3.813	31.778	+
7+	28.3	A/N	80x25	Mono	6.356	25.422	0.636	1.907	3.813	31.778	+
D	25.2	APA	320x200	16	6.356	25.422	0.636	1.907	3.813	31.778	-
E	25.2	APA	640x200	16	6.356	25.422	0.636	1.907	3.813	31.778	-
F	25.2	APA	640x350	Mono	6.356	25.422	0.636	1.907	3.813	31.778	+
10	25.2	APA	640x350	16	6.356	25.422	0.636	1.907	3.813	31.778	+
11	25.2	APA	640x480	2	6.356	25.422	0.636	1.907	3.813	31.778	-
12	25.2	APA	640x480	16	6.356	25.422	0.636	1.907	3.813	31.778	-
13	25.2	APA	320x200	256	6.356	25.422	0.477	2.066	3.813	31.778	-
50	25.2	A/N	80x30	16	6.356	25.422	0.636	1.907	3.813	31.778	-
51	25.2	A/N	80x43	16	6.356	25.422	0.636	1.907	3.813	31.778	-
52	25.2	A/N	80x60	16	6.356	25.422	0.636	1.907	3.813	31.778	-
53	40.0	A/N	132x25	16	5.600	26.400	0.000	1.800	3.800	32.000	+
54	40.0	A/N	132x30	16	5.600	26.400	0.000	1.800	3.800	32.000	-
55	40.0	A/N	132x43	16	5.600	26.400	0.000	1.800	3.800	32.000	-
56	40.0	A/N	132x60	16	5.600	26.400	0.000	1.800	3.800	32.000	-
57	44.9	A/N	132x25	16	5.612	26.459	-0.200	1.804	4.009	32.071	+
58	44.9	A/N	132x30	16	5.612	26.459	-0.200	1.804	4.009	32.071	-
59	44.9	A/N	132x43	16	5.612	26.459	-0.200	1.804	4.009	32.071	-
5A	44.9	A/N	132x60	16	5.612	26.459	-0.200	1.804	4.009	32.071	-
5B	36.0	APA	800x600	16	6.222	22.222	0.667	3.500	2.028	28.660	-
5B[1]	50.35	APA	800x600	16	4.926	15.889	0.794	2.066	2.066	20.814	+
5C[1]	50.35	APA	640x400	256	6.356	25.422	0.556	1.668	4.131	31.778	-
5D[1]	50.35	APA	640x480	256	6.356	25.422	0.556	1.668	4.131	31.778	-
5E	57.3	APA	800X600 (I)	256	5.587	27.937	0.139	1.676	3.771	33.574	-
5E[1]	72.0	APA	800x600	256	6.222	22.222	0.667	3.500	2.028	28.660	-
5F	44.9	APA	1024x768 (I)	16	5.345	22.806	0.204	1.260	3.956	28.151	+
5F	65.0	APA	1024x768 (NI)	16	4.800	15.754	0.615	1.108	3.077	20.554	+
5F[1]	75.0	APA	1024X768 (NI)	16	4.053	13.653	0.320	1.920	1.813	17.707	+
60	44.9	APA	1024X768(I)	4	5.345	22.806	1.069	1.782	2.494	28.151	+
61	44.9	APA	768x1024 (I)	16	9.265	17.105	-1.782	4.633	4.811	26.370	+

[1]Based on VESA (Video Electronics Standards Association) standards VS900502 and VS910801.

Table 10-b. Vertical Timing (msec)

MODE	CLK	TYPE	DISPLAY COLORS	MAX	T1	T2	T3	T 4	T5	POLARITY
0,1	25.2	A/N	40x25	16	1.577	12.711	0.413	14.268	0.064	+
2,3	25.2	A/N	80x25	16	1.577	12.711	0.413	14.268	0.064	+
0*,1*	25.2	A/N	40x25	16	3.146	11.122	1.208	14.268	0.064	-
2*,3*	25.2	A/N	80x25	16	3.146	11.122	1.208	14.268	0.064	-
0+,1+	28.3	A/N	40x25	16	1.577	12.711	0.413	14.268	0.064	+
2+,3+	28.3	A/N	80x25	16	1.577	12.711	0.413	14.268	0.064	+
4,5	25.2	APA	320x200	4	1.577	12.711	0.413	14.268	0.064	+
6	25.2	APA	640x200	2	1.577	12.711	0.413	14.268	0.064	+
7	28.3	A/N	80x25	Mono	3.146	11.122	1.208	14.268	0.064	+
7+	28.3	A/N	80x25	Mono	1.577	12.711	0.413	14.268	0.064	+
D	25.2	APA	320x200	16	1.577	12.711	0.413	14.268	0.064	+
E	25.2	APA	640x200	16	1.577	12.711	0.413	14.268	0.064	+
F	25.2	APA	640x350	Mono	3.146	11.122	1.208	14.268	0.064	-
10	25.2	APA	640x350	16	3.146	11.122	1.208	14.268	0.064	-
11	25.2	APA	640x480	2	1.430	15.253	0.350	16.683	0.064	-
12	25.2	APA	640x480	16	1.430	15.253	0.350	16.683	0.064	-
13	25.2	APA	320x200	256	1.577	12.711	0.413	14.268	0.064	+
50	25.2	A/N	80x30	16	1.430	15.253	0.350	16.683	0.064	-
51	25.2	A/N	80x43	16	1.652	15.031	0.540	16.683	0.064	-
52	25.2	A/N	80x60	16	1.430	15.253	0.350	16.683	0.064	-
53	40.0	A/N	132x25	16	3.168	11.200	1.248	14.368	0.064	-
54	40.0	A/N	132x30	16	1.376	15.360	0.352	16.736	0.064	-
55	40.0	A/N	132x43	16	1.600	15.136	0.576	16.736	0.064	-
56	40.0	A/N	132x60	16	1.376	15.360,	0.352	16.736	0.064	-
57	44.9	A/N	132x25	16	3.079	11.225	1.219	14.304	0.064	-
58	44.9	A/N	132x30	16	1.315	15.394	0.321	16.709	0.064	-
59	44.9	A/N	132x43	16	1.539	15.170	0.417	16.709	0.064	-
5A	44.9	A/N	132x60	16	1.315	15.394	0.321	16.709	0.064	-
5B	36.0	APA	800x600	16	0.711	17.067	0.028	17.715	0.057	-
5B[2]	50.35	APA	800x600	16	1.395	12.489	0.479	13.883	0.125	+
5C[1]	50.35	APA	640x400	256	1.557	12.711	0.413	14.268	0.064	+
5D	50.35	APA	640x480	256	1.430	15.253	0.350	16.683	0.064	-
5E	57.3	APA	800x600 (I)	256	1.073	10.057	0.151	11.130	0.067	-
5E[1]	72.0	APA	800x600	256	0.711	17.067	0.028	17.778	0.057	-
5F	44.9	APA	1024x768 (I)	16	0.873	10.810	0.155	11.683	0.056	+
5F	65.0	APA	1024x768 (NI)	16	0.945	15.785	0.329	16.731	0.041	+
5F[1]	75.0	APA	1024X768 (NI)	16	0.673	13.599	0.053	14.272	0.106	+
60	44.9	APA	1024X768(I)	4	0.873	10.810	0.155	11.683	0.056	+
61	44.9	APA	768x1024 (I)	16	0.791	13.501	0.119	14.292	0.040	+

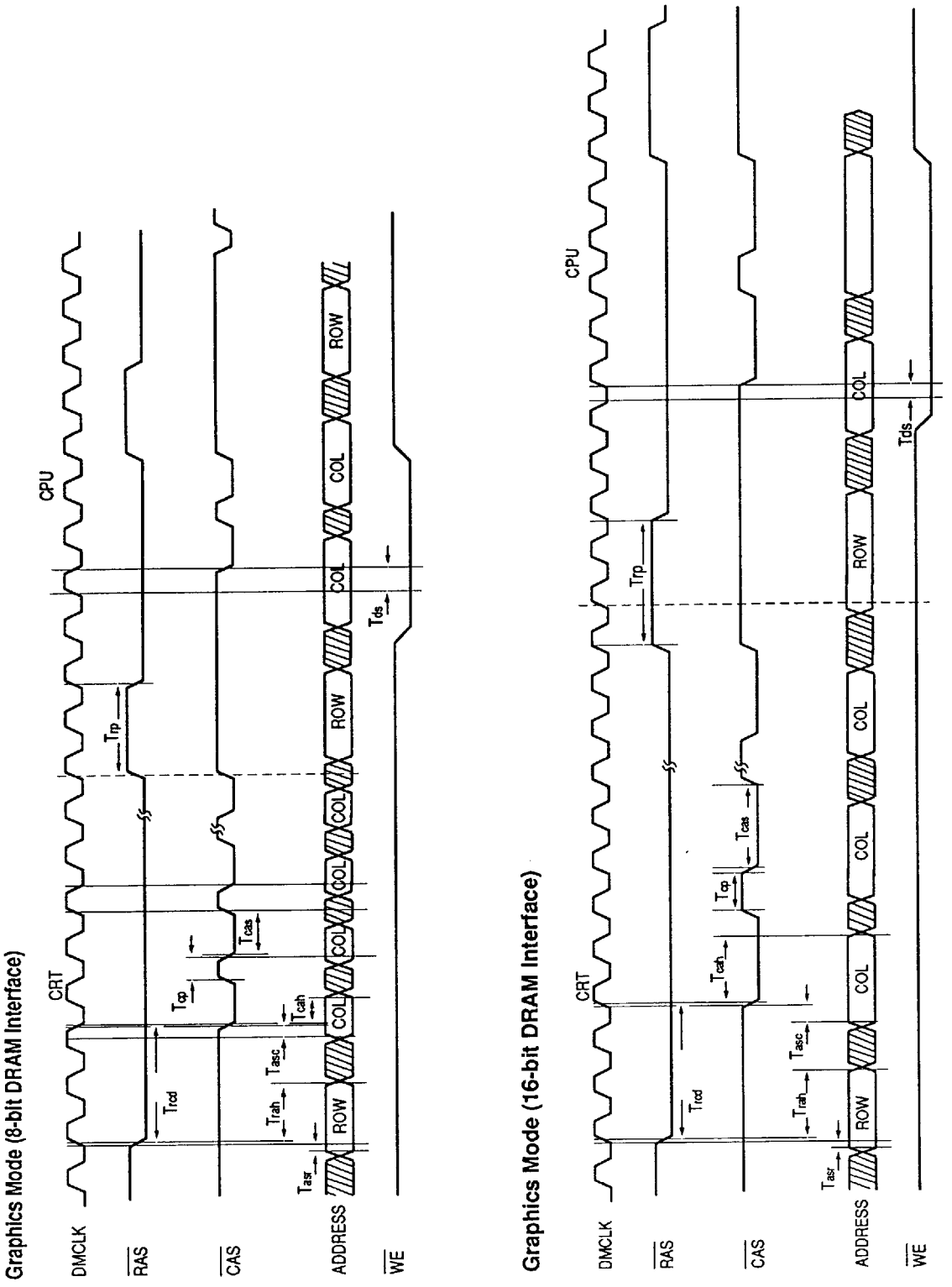

Figure 7a. Trident TVGA9000I DRAM Timing (Graphics)

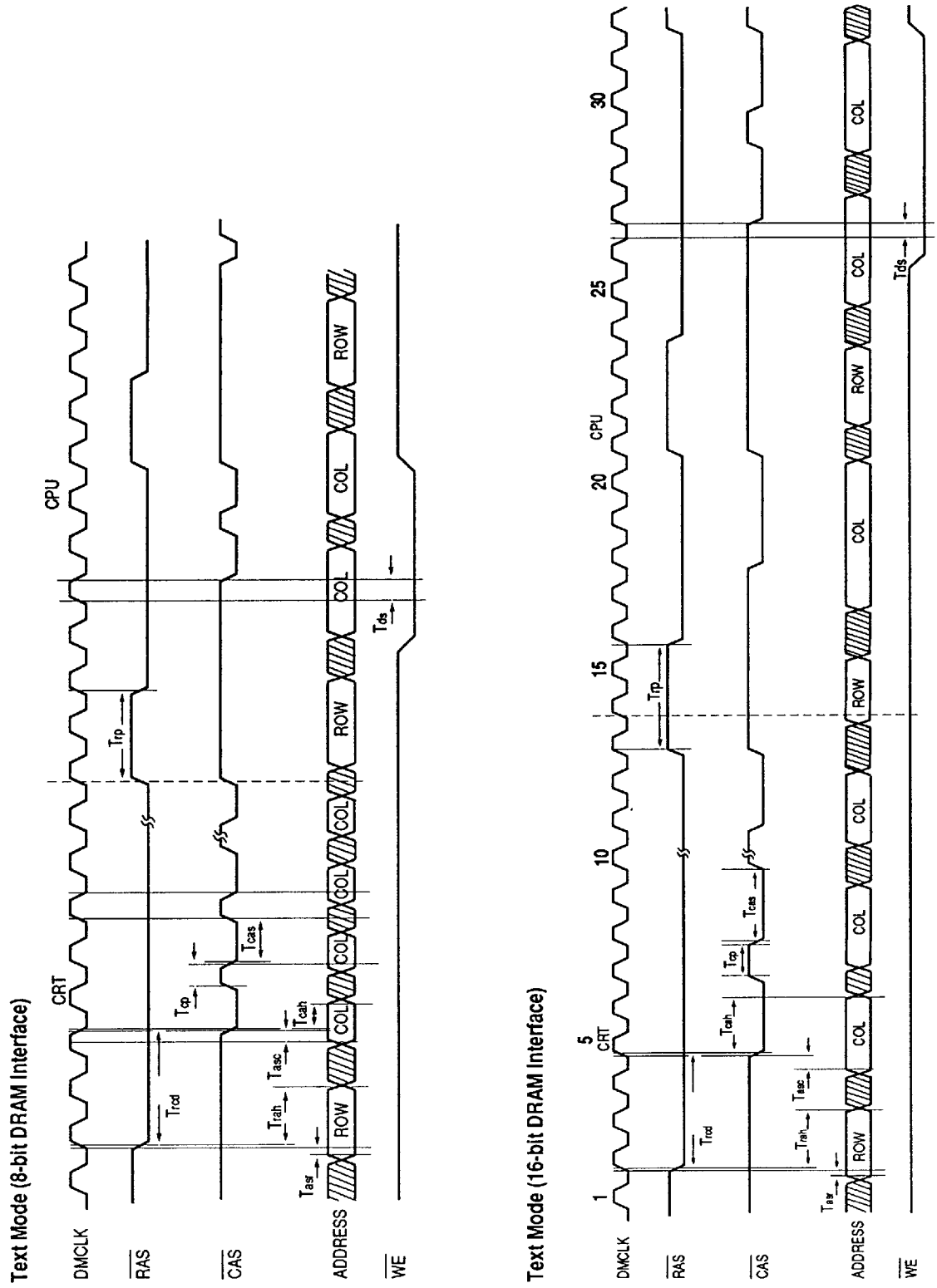

Figure 7b. Trident TVGA9000I DRAM Timing (Text)

Table 11. Worst Case Memory Timing Parameters[1]

Parameter	2 DRAM	4 DRAM
Trcd 1	2.5t + 2	3t
Trah 2	1.5t + 3	2t
Tasr 3	≥ 0	≥ 0
Tasc 4	≥ t	≥ t
Tcah 5	t + 6	2t + 10
Tcp 6	0.5t + 2	t + 1
Tcas 7	t	2t
Tds 8	≥ 0	≥ 0
Trp 9	2t	3t + 10
Test Load	25pf	50pf

[1] t=1/DMCLK

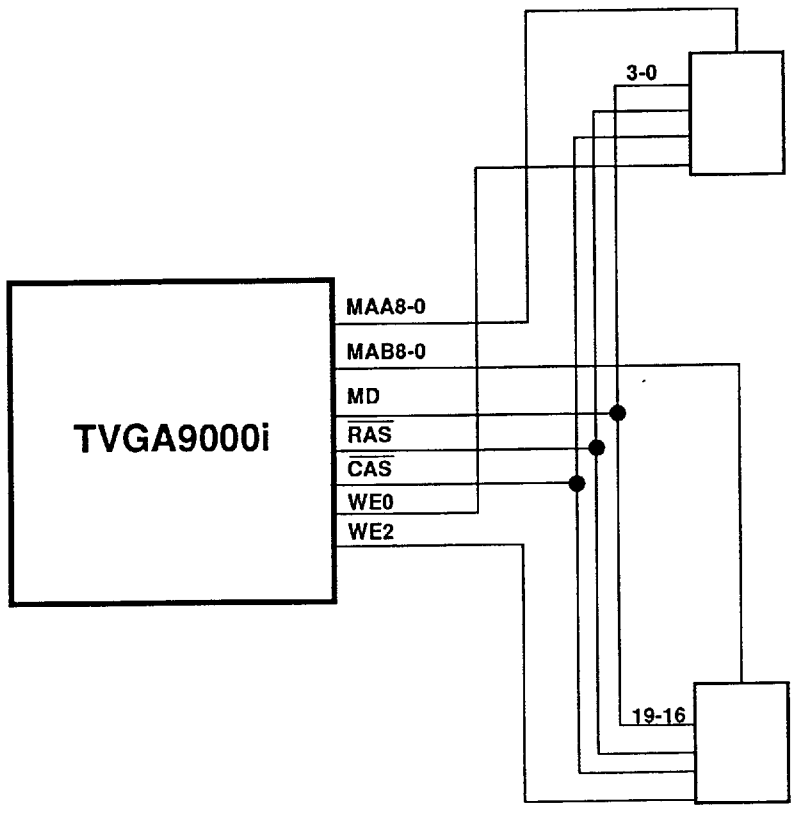

Figure 8a. Standard Application for Two 256Kx4 DRAM

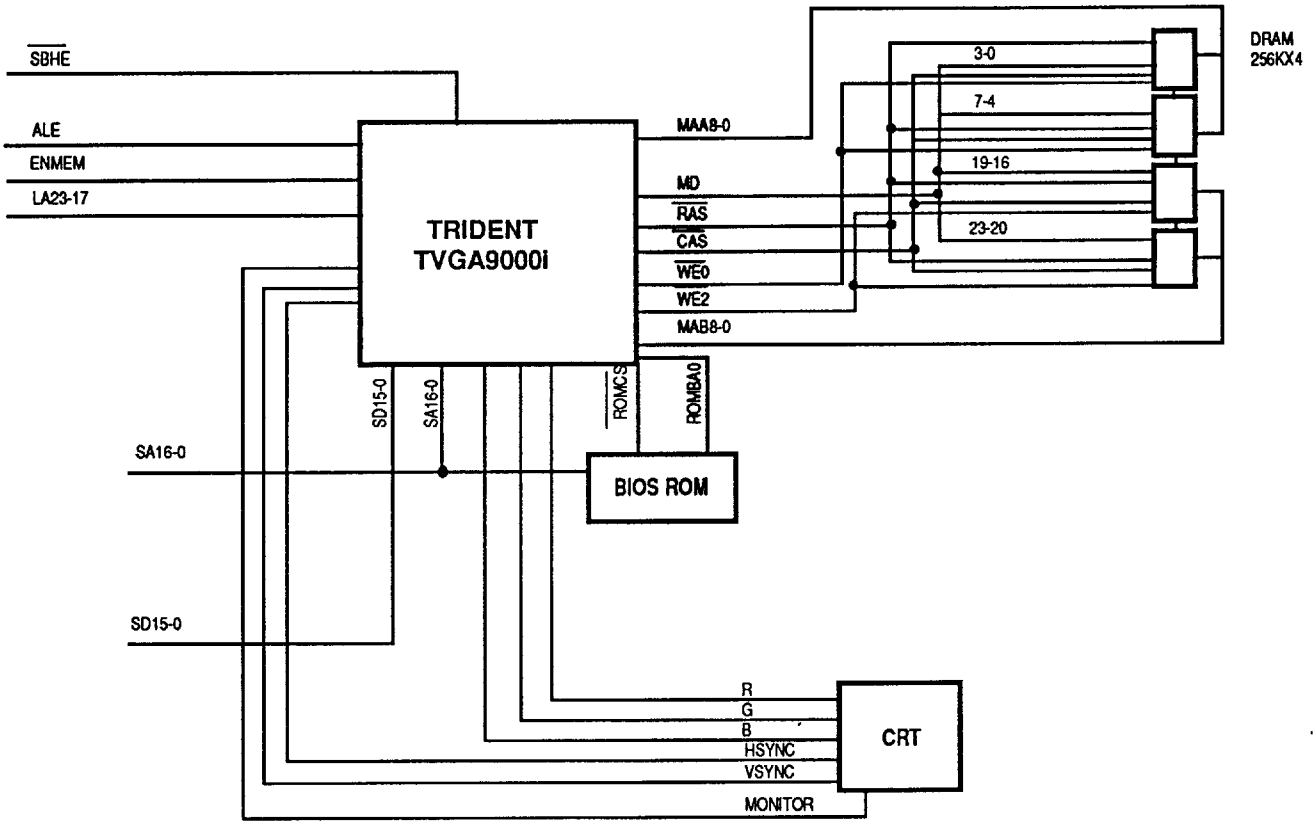

Figure 8b. Standard Application for Four 256Kx4 DRAM

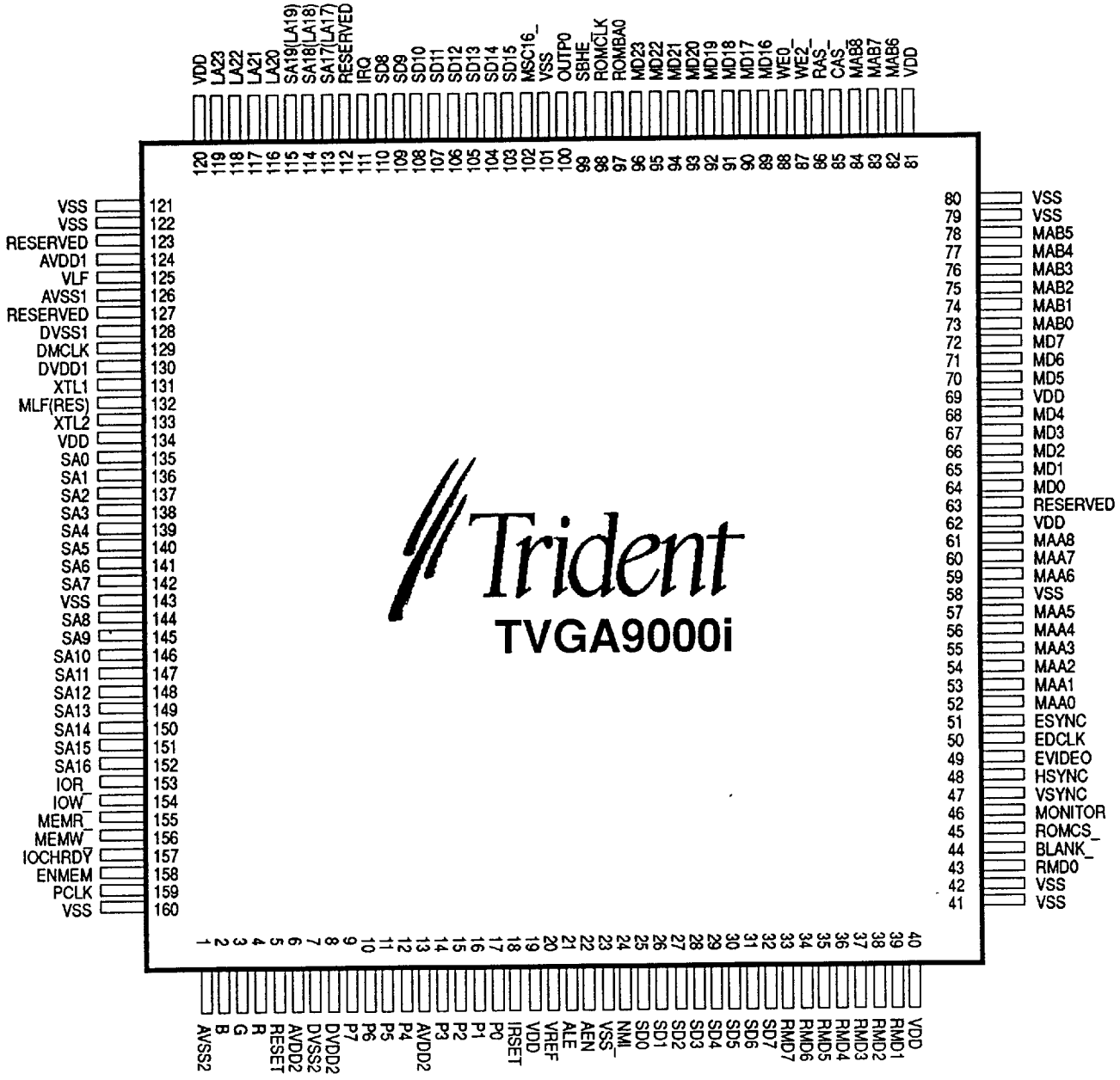

Figure 9. TVGA9000I ISA Pin-Out

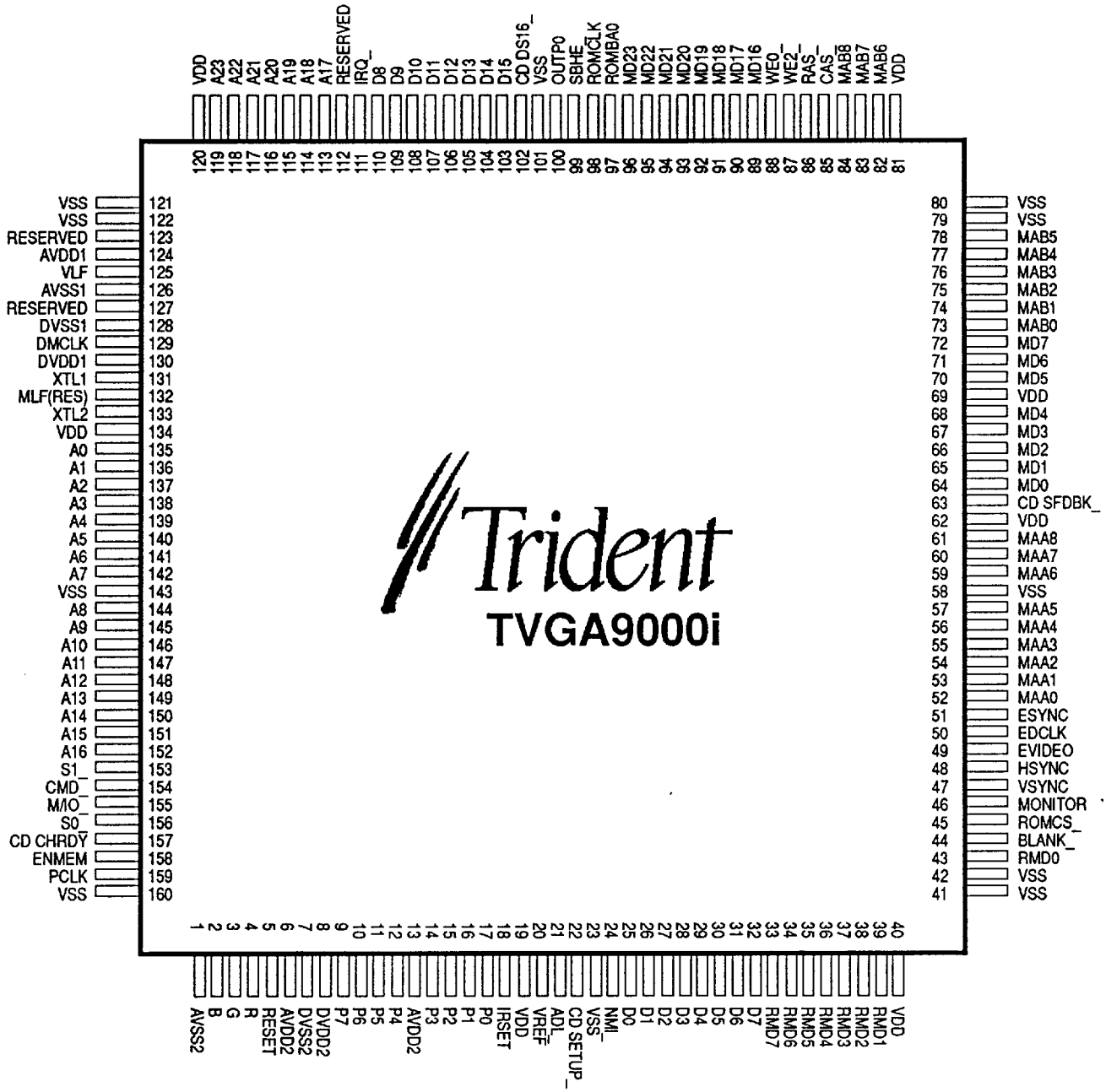

Figure 10. TVGA9000i MCA Pin-Out

Table 12. TVGA9000i Pin Description

Pin	Pin Type	Pin Number	Description
Host Interface			
a. AT Bus Signals			
$\overline{IOR}$	I	153	I/O read strobe
$\overline{IOW}$	I	154	I/O write strobe
$\overline{MEMR}$	I	155	Memory read strobe
$\overline{MEMW}$	I	156	Memory write strobe
IOCHRDY	O	157	I/O channel ready
ALE	I	21	System address latch enable
AEN	I	22	Enable on-board I/O
LA23-LA20	I	119-116	Unlatched address bus, bit 23 to bit 20
SA19-SA17 (LA19-LA17)	I	115-113	Address bus, bit 19 to bit 17 (Unlatched address bus, bit 19 to bit 17)
SA16-SA0	I/O	152-144,142-135	Address Bus
$\overline{MCS16}$	O	102	Enable 16-bit transfer, open drain output
SD15-SD0	I/O	103-110,32-25	Data bus (high byte), bit 15 to bit 0
IRQ	O	111	Interrupt request
b. MCA Bus Signals			
$\overline{S1-S0}$	I	153,156	Status bit 1-0
$\overline{CMD}$	I	154	Command
M/$\overline{IO}$	I	155	Bus memory or I/O cycle
CD CHRDY	O	157	Channel ready
$\overline{ADL}$	I	21	System address latch enable
$\overline{CD\ SETUP}$	I	22	Card setup
A23-A0	I	119-113,152-144,142-135	System address bus, bit 23 to bit 0
$\overline{CD\ DS16}$	O	102	Card data size 16-bit
D15-D0	I/O	103-110,32-25	System data bus, bit 15 to bit 0
$\overline{CD\ SFDBK}$	O	63	Card select feedback
$\overline{IRQ}$	O	111	Interrupt request
Common Bus Signals			
RESET	I	5	System reset (active high); the falling edge latches configuration information into internal registers from memory data lines and AD7-AD0
$\overline{NMI}$	O	24	Non-maskable interrupt, open-drain output
$\overline{SBHE}$	I	99	Bus high-byte enable
ENMEM	I	158	Enable display memory

continued on next page

Table 12. TVGA9000i Pin Description - continued

Pin	Pin Type	Pin Number	Description
Display Memory Interface			
CAS	O	85	Column address strobe
RAS	O	86	Row address strobe
WE2	O	87	Write enable
WE0	O	88	Write enable
MAA8-MAA0	O	61-59, 57-52	Multiplexing address bus of display memory Bank A
MAB8-MAB0	O	84-82,78-73	Multiplexed address bus of display memory Bank B
MD23-MD16	I/O	96-89	Memory data bus (bit 23 to bit 16)
MD7-MD0	I/O	72-70, 68-64	Memory data bus (bit 7 to bit 0)
DMCLK	I/O	129	DRAM clock (for test use)
Video Interface			
VSYNC	O	47	Vertical synchronization pulse, polarity programmable
HSYNC	O	48	Horizontal synchronization pulse, polarity programmable
RMD7-RMD0	I/O	33-39,43	ROM/DAC data bus, bit 7 to bit 0
B	O	2	Blue output
G	O	3	Green output
R	O	4	Red output
IRSET	I	18	Full-scale RGB output voltage adjust control
VREF	I	20	External voltage reference pin
P7-P0	I/O	9-12, 14-17	Pixel data address bits 7-0 from feature connector or to feature connector
PCLK	I/O	159	Pixel clock input from feature connector or to feature connector
BLANK	I/O	44	Blank input from feature connector or to feature connector
ESYNC	I	51	External sync enabled (Feature connector) 1: allows HSYNC, VSYNC to feature connector 0: disables HSYNC, VSYNC
EDCLK	I	50	External pixel clock enabled (Feature connector) 1: allows PCLK to feature connector 0: disables PCLK
EVIDEO	I	49	External pixel data enabled (Feature connector) 1: allows P[7-0] to feature connector 0: disables P[7-0]
Clock Synthesizer Interface			
XTL1	O	131	Crystal output, connect to 40MHz crystal
XTL2	I	133	Crystal input, connect to 40MHz crystal

continued on next page

Table 12. TVGA9000i Pin Description - continued

Pin	Pin Type	Pin Number	Description
BIOS Interface			
ROMCS	O	45	BIOS EPROM chip select
ROMBA0	O	97	BIOS EPROM address bit 14
ROMCLK	I	98	ROM wait state clock
Other External Interfaces			
MONITOR	I	46	Monitor type detect (analog monitors)
VLF	O	125	Filter node output
OUTP0	O	100	Programmable output 0
Reserved Pins			
MLF(RES)	O	132	Reserved
RESERVED	NA	112, 123, 127	Reserved for chip testing
Power Pins			
AVSS2	GND	1	Ground for display DAC (analog section)
AVSS1	GND	126	Ground for Clock Synthesizer (analog section)
DVSS2	GND	7	Ground for display DAC (digital section)
DVSS1	GND	128	Ground for Clock Synthesizer (digital section)
AVDD2	PWR	6,13	Power for display DAC (analog section)
AVDD1	PWR	124	Power for Clock Synthesizer (analog section)
DVDD2	PWR	8	Power for display DAC (digital section)
DVDD1	PWR	130	Power for Clock Synthesizer (digital section)
VSS	GND	23,41,42,58,79,80,101 121,122, 143, 160	Ground
VDD	PWR	19,40,62, 69, 81,120,134	+5VDC

[1]Pins definition in parentheses are for linear addressing

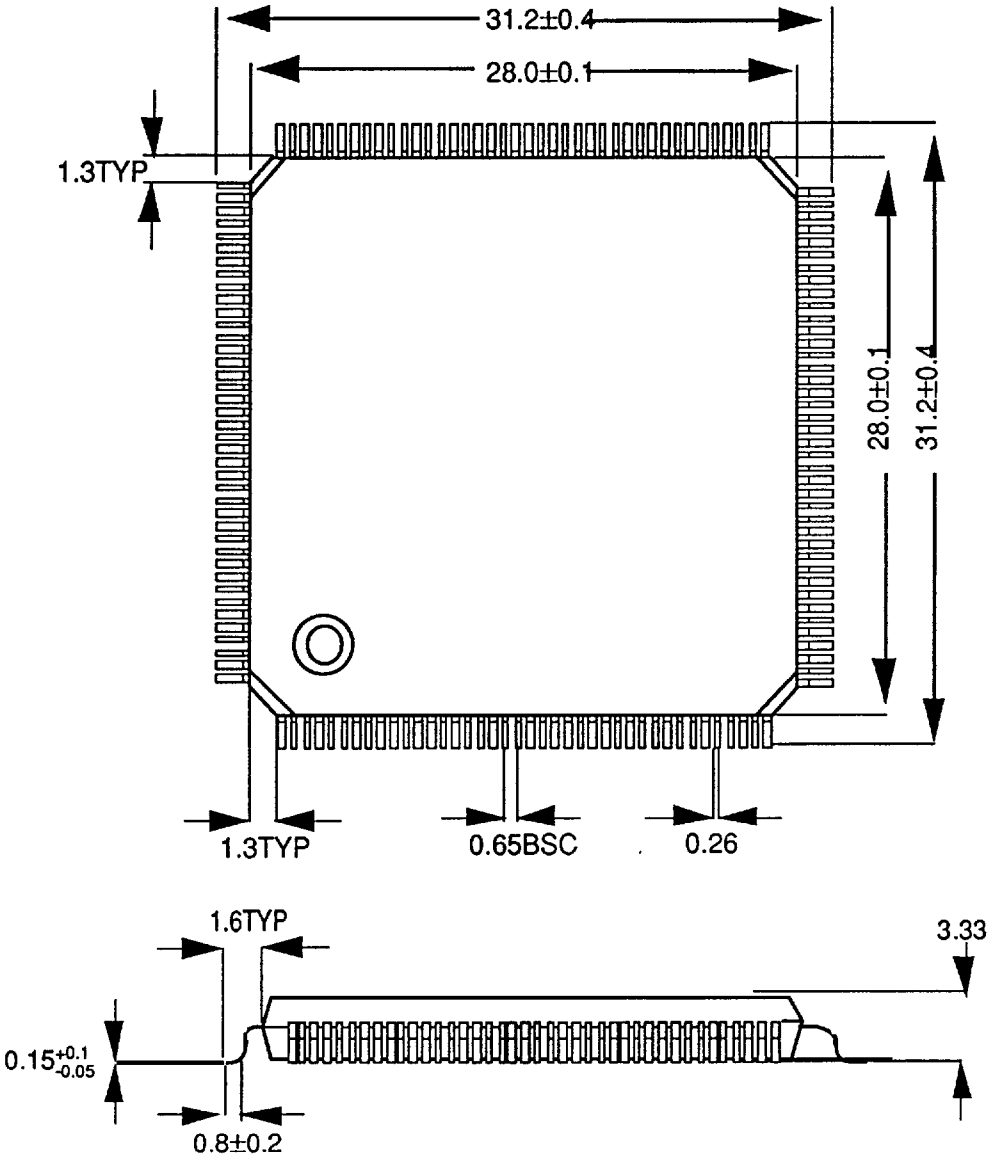

Figure 11. TVGA9000i Packaging PFP 160 Pins